

# Diseño de un sistema operativo de disco

(Por Primitivo de Francisco y Jesús Alonso)

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B

1

DIRECCION REAL PAGINADA → 0000

DOS V 2.3

(23755) 5CCB } 112 BYTES  
(23867) 5D3B

ZONA DESPLAZADA DE PROG

IMPRESION →

IMPRESION TEXTO →

```

A000 F3 DI
A001 11FFFF LD DE,FFFF
A004 3E07 LD A,07
A006 1801 JR A009
A008 00 NOP
A009 00FE OUT (FE),A
A00B 3E07 LD A,07
A00D 1804 JR A013
A00F 00 NOP
A010 C3013D JP 3D01
A013 ED47 LD I,A
A015 00 NOP
A016 1803 JR A018
A018 C30F3D JP 3D0F
A01E 00 NOP
A01F 00 NOP
A020 00 LD H,D
A021 00 LD L,E
A022 00 LD (HL),02
A023 00 DEC HL
A024 00 CP H
A025 00 JR NZ,A020
A026 00 OR A
A027 00 SBC HL,DE
A028 00 ADD HL,DE
A029 00 INC HL
A02A 00 JR NC,A033
A02B 00 DEC (HL)
A02C 00 JR Z,A033
A02D 00 DEC (HL)
A02E 00 JR Z,A026
A02F 00 DEC HL
A030 00 LD (5C84),HL
A031 00 LD DE,3EAF
A032 00 LD BC,00A8
A033 00 LD A,E
A034 00 EX DE,HL
A035 00 LD SP,5000
A036 00 CALL 3CF1
A037 00 EX DE,HL
A038 00 INC HL
A039 00 LD (5C7B),HL
A03A 00 DEC HL
A03B 00 LD BC,1E40
A03C 00 LD (5C80),BC
A03D 00 LD (5C82),HL
A03E 00 LD HL,3C00
A03F 00 LD (5C86),HL
A040 00 LD HL,(5C82)
A041 00 LD (HL),3E
A042 00 DEC HL
A043 00 LD SP,HL
A044 00 DEC HL
A045 00 DEC HL
A046 00 LD (5C3D),HL
A047 00 LD DE,1303
A048 00 PUSH DE
A049 00 IM 1
A04A 00 LD IY,5C3A
A04B 00 LD HL,5C86
A04C 00 LD (5C4F),HL
A04D 00 LD DE,15AF
A04E 00 LD BC,0015
A04F 00 EX DE,HL
A050 00 CALL 3CF8
A051 00 EX DE,HL
A052 00 DEC HL
A053 00 LD (5C57),HL
A054 00 INC HL
A055 00 LD (5C53),HL
A056 00 LD (5C4B),HL
A057 00 LD (HL),80
A058 00 INC HL
A059 00 LD (5C59),HL
A05A 00 CALL 02B7
A05B 00 INC HL
A05C 00 LD (5C61),HL
A05D 00 LD (5C63),HL
A05E 00 LD (5C65),HL
A05F 00 LD A,38
A060 00 LD (5C8D),A
A061 00 LD (5C8F),A
A062 00 LD (5C48),A
A063 00 LD HL,0523
A064 00 LD (5C89),HL
A065 00 DEC (IY+C8)
A066 00 DEC (IY+C9)
A067 00 LD HL,1506
A068 00 LD DE,5C10
A069 00 LD BC,000E
A06A 00 CALL 3CF8
A06B 00 SET 1,(IY+01)
A06C 00 LD HL,0EDF
A06D 00 CALL 0ABE
A06E 00 LD HL,5C6B
A06F 00 LD (HL),02
A070 00 LD HL,1285
A071 00 PUSH HL
A072 00 JP 3D79

```

BORDE BLANCO

PRMT

ULG

RASP

RAMTOP

CHARS

ERR-SP

ERR-NR

FUERA

CHANS

DORND

PROG

VALC

ELINE

WORKSP

STK BOT

STKEND

ATLTP

ATLTL

BORDCR

REPEL

STRMS

DEFSZ

```

A0000 CD2130 CALL 3D21
A0001 CD18D0 CALL 018D
A0002 CD0850 CALL 085B
A0003 CD0850 LD HL, (5C59) ELINE
A0004 CD0850 LD A, (HL)
A0005 CD0850 CP AA
A0006 CD0850 JR NZ, A0F1
A0007 CD0850 INC HL
A0008 CD0850 LD E, (HL)
A0009 CD0850 INC HL
A0010 CD0850 LD D, (HL)
A0011 CD0850 EX DE, HL
A0012 CD0850 JR A0F4
A0013 CD0850 LD HL, 0001
A0014 CD0850 LD (5C42), HL NEWPPC
A0015 CD0850 XOR A
A0016 CD0850 LD (5C44), A NSPPC
A0017 CD0850 LD HL, 1550
A0018 CD0850 CALL 085E
A0019 CD0850 LD HL, (5C53) PR0G
A0020 CD0850 DEC HL
A0021 CD0850 LD (5C57), HL DATA0D
A0022 CD0850 LD HL, 3C15
A0023 CD0850 CALL 085E
A0024 CD0850 CALL 3D21
A0025 CD0850 LD A, FF
A0026 CD0850 LD (5D15), A STANS
A0027 CD0850 XOR A
A0028 CD0850 LD (5C77), A
A0029 CD0850 CALL 3D8E
A0030 CD0850 LD A, AA
A0031 CD0850 LD (5D17), A
A0032 CD0850 LD HL, 017E
A0033 CD0850 LD (5D1A), HL
A0034 CD0850 LD HL, 0000
A0035 CD0850 ADD HL, SP
A0036 CD0850 LD (5D1C), HL
A0037 CD0850 DEC HL
A0038 CD0850 DEC HL
A0039 CD0850 LD SP, HL
A0040 CD0850 CALL 0185
A0041 CD0850 LD HL, (5C5D) CHADD
A0042 CD0850 CALL 0155
A0043 CD0850 JP NZ, 015E
A0044 CD0850 CP EA
A0045 CD0850 INC HL
A0046 CD0850 JR NZ, A138
A0047 CD0850 CALL 0155
A0048 CD0850 JR NZ, A13B
A0049 CD0850 CP 3A
A0050 CD0850 JP NZ, 015E
A0051 CD0850 INC HL
A0052 CD0850 LD A, (HL)
A0053 CD0850 LD (5D11), HL
A0054 CD0850 JP 021F
A0055 7E LD A, (HL)
A0056 7E80 CP 80
A0057 08 RET NZ
A0058 7E80 CP 80
A0059 08 RET Z
A0060 0B OR I
A0061 0B RET
A0062 CD0850 CALL 3D21
A0063 3A175D LD A, (5D17)
A0064 B7 OR A
A0065 2803 JR NZ, A16A
A0066 CD0850 CALL 3E75
A0067 CD0850 CALL 0859
A0068 CD0850 CALL 019D
A0069 CD0850 LD SP, (5D1C)
A0070 CD0850 LD HL, (5D1A)
A0071 CD0850 LD BC, (5D0F)
A0072 CD0850 LD B, 00
A0073 CD0850 JP HL
A0074 CD0850 CALL 018C
A0075 FDC8007E BIT 7, (IY+00)
A0076 C0 RET NZ
A0077 2A635C LD HL, (5C63) STK0T
A0078 2A655C LD (5C65), HL STK0D
A0079 E5 PUSH HL
A0080 2A1925C LD HL, 5C92
A0081 2E685C LD (5C68), HL
A0082 E1 POP HL
A0083 11E53C LD DE, 3CBE
A0084 ED783D5C LD SP, (5C3D) ERRSP
A0085 05 PUSH DE
A0086 C9 RET
A0087 CD0850 CALL 08AE
A0088 F800 CP 00
A0089 C8 RET Z
A0090 CD0850 CALL 086F
A0091 1878 JR A18D
A0092 2A3D5C LD HL, (5C3D) ERRSP
A0093 2A135D LD (5D13), HL
A0094 2A105D LD HL, (5D1C) STANS
A0095 2E DEC HL
A0096 2E DEC HL
A0097 2A3D5C LD (5C3D), HL
A0098 110F3C LD DE, 3C0F
A0099 73 LD (HL), E
A0100 2E INC HL
A0101 7E LD (HL), D
A0102 C9 RET

```

CALCULA BYTES LIBRES ?

```

R1100 LD HL,(5D13)
R1101 LD (5C3D),HL
R1102 RET
R1103 LD HL,0000
R1104 LD (5CF7),HL
R1105 ADD HL,SP
R1106 LD (5D1C),HL
R1107 DEC HL
R1108 DEC HL
R1109 LD SP,HL
R1110 CALL 01A8
R1111 LD HL,5D17
R1112 LD A,(HL)
R1113 JP Z,01F1
R1114 LD (HL),A
R1115 CALL 0A8B
R1116 CALL 0A8A
R1117 LD HL,0277 → FICHERO MENSAJE INICIAL
R1118 RST 18 0269
R1119 LD HL,0264 → RESID DEL MENSAJE (QUITAR 2ª PARTE DEL MENSAJE)
R1120 RST 18
R1121 CALL 3DAB → PREPARA CONTROLADOR
R1122 CALL 026F → PREGUNTA CLAVE
R1123 LD HL,(5D1C)
R1124 DEC HL
R1125 DEC HL
R1126 LD SP,HL
R1127 CALL 3D21 → CANAL 0
R1128 CALL 0A84 → CANAL 0
R1129 CALL 3E50 → RUTINA AUTOMODIFICACION
R1130 XOR A
R1131 LD (5D15),A
R1132 LD HL,01F1
R1133 LD (5D1A),HL
R1134 CALL 3DAB →
R1135 CALL 3D4C →
R1136 XOR A
R1137 LD (5D0F),A
R1138 LD HL,(5C59)
R1139 LD (5D11),HL
R1140 LD A,(HL)
R1141 CP 0D
R1142 JR Z,A200
R1143 LD HL,(5D1F)
R1144 DEC HL
R1145 LD C,00
R1146 INC C
R1147 LD D,A
R1148 LD A,(5D23)
R1149 CP C
R1150 JP C,015E
R1151 LD A,D
R1152 INC HL
R1153 CP (HL)
R1154 JR NZ,A225
R1155 XOR A
R1156 LD (5D0F),A
R1157 LD (3C06),A
R1158 LD (5D10),A
R1159 LD HL,5C3B
R1160 RES 7,(HL)
R1161 LD B,00
R1162 LD HL,(5D21)
R1163 DEC C
R1164 SLA C
R1165 ADD HL,BC
R1166 LD E,(HL)
R1167 INC HL
R1168 LD D,(HL)
R1169 EX DE,HL
R1170 PUSH HL
R1171 LD DE,0255
R1172 PUSH DE
R1173 JP HL
R1174 LD HL,5C3B
R1175 SET 7,(HL)
R1176 POP HL
R1177 JP HL
R1178 CALL 0A86
R1179 CALL 034D
R1180 LD HL,3F03 → NUEVE CLAVE
R1181 RST 18
R1182 CALL 02CF
R1183 LD DE,555A → DESTINO
R1184 LD HL,5C06 → ORIGEN
R1185 LD BC,0009 → N°
R1186 LDIR
R1187 JP 3D1E

```

16 01 03 1401 -- b.o.l. 72 1480  
DF

NUEVE CLAVE

RECIBO EL N.º DE CLAVE

↑  
TEXTO DE CABECERA

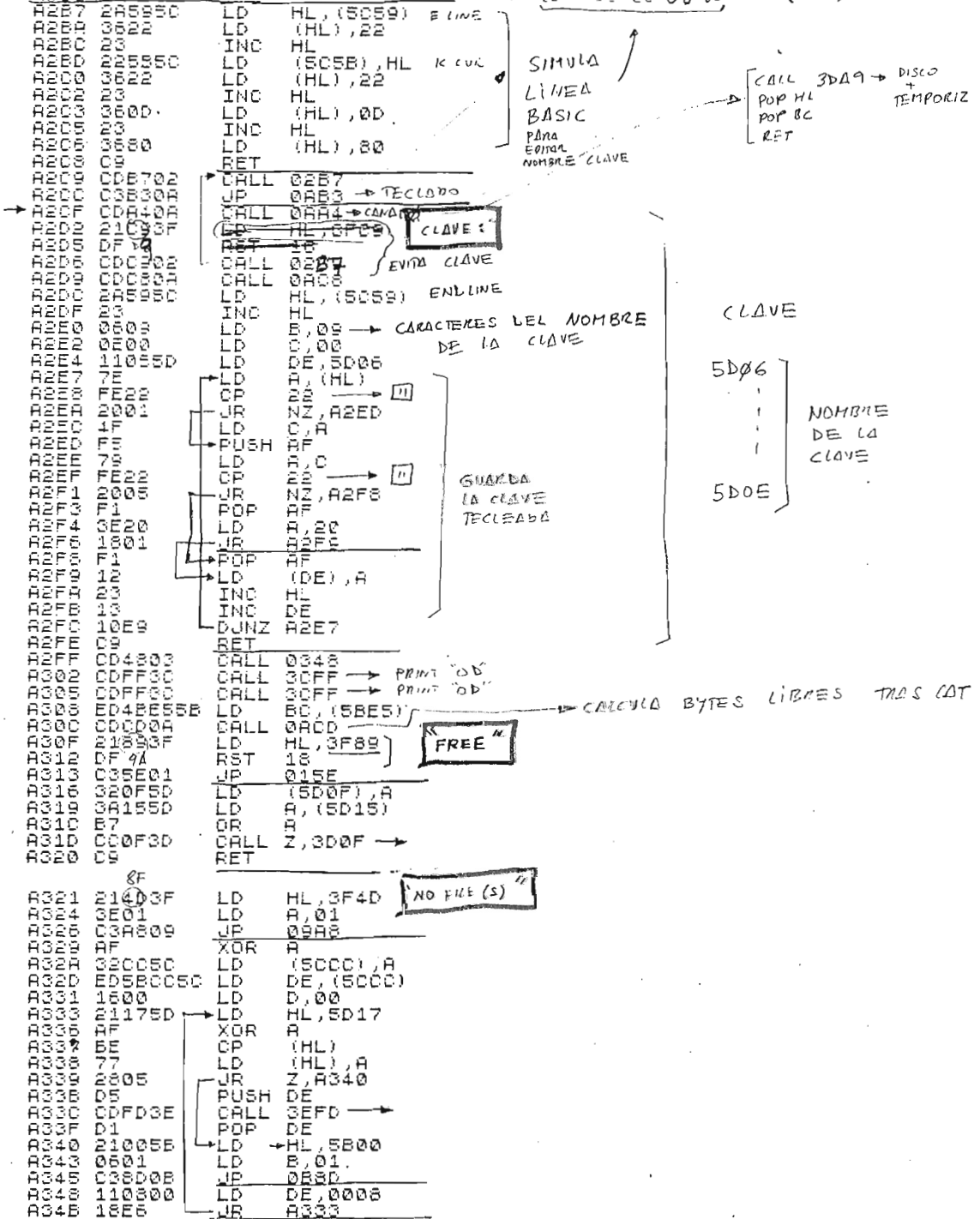
```

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H00FF 0000 0000 0000

```

TABLA CON EL TEXTO

2B RESISTIVE LO  
 22 3D 5C MODIFICADO EN  
 11 03 13 0066  
 C3 64 00 RESTO DE  
 CODIGO PARA  
 LA MODIFICACION  
 (NMI)



```

A300 004800  CALL 0348
A301 004801  LD A, (5BE7)
A302 004802  CP 07
A303 004803  JNR Z, A361
A304 004804  CP 0A
A305 004805  JNR Z, A361
A306 004806  LD HL, 3F9E
A307 004807  RST 18
A308 004808  JR A313
A309 004809  LD BC, (5CFE)
A310 004810  LD HL, 5004
A311 004811  ADD HL, BC
A312 004812  LD (HL), A
A313 004813  LD A, (5BE3)
A314 004814  INC HL
A315 004815  INC HL
A316 004816  INC HL
A317 004817  LD (HL), A
A318 004818  LD HL, 5006
A319 004819  LD DE, 5BEA
A320 004820  LD B, 09
A321 004821  CALL 30BE
A322 004822  RET Z
A323 004823  CALL 02CF
A324 004824  JR A340
A325 004825  LD HL, (5D11)
A326 004826  INC HL
A327 004827  LD A, (HL)
A328 004828  CP 0D
A329 004829  JNR Z, 039A
A330 004830  CALL 0800
A331 004831  CALL 0A95
A332 004832  CALL 0AD2
A333 004833  EX DE, HL
A334 004834  CALL 09DE
A335 004835  CALL 0A95
A336 004836  CALL 0340
A337 004837  CALL 0A8B
A338 004838  CALL 0AAA
A339 004839  LD HL, 3FB8
A340 004840  RST 18
A341 004841  LD HL, 5BF8
A342 004842  RST 18
A343 004843  CALL 30FF
A344 004844  LD A, (5BE4)
A345 004845  LD HL, 5BF4
A346 004846  SUB (HL)
A347 004847  PUSH HL
A348 004848  CALL 3EBA
A349 004849  LD HL, 3F50
A350 004850  RST 18
A351 004851  POP HL
A352 004852  LD C, (HL)
A353 004853  CALL 3EBB
A354 004854  LD HL, 3F59
A355 004855  RST 18
A356 004856  CALL 0329
A357 004857  LD HL, 5B00
A358 004858  CALL 3EE5
A359 004859  CALL 30FF
A360 004860  LD A, (5CFE)
A361 004861  ADD A, 41
A362 004862  RST 18
A363 004863  LD B, 02
A364 004864  CALL 3EE5
A365 004865  PUSH BC
A366 004866  LD A, 3A
A367 004867  RST 18
A368 004868  PUSH HL
A369 004869  CALL 3076
A370 004870  LD BC, 000D
A371 004871  POP HL
A372 004872  PUSH HL
A373 004873  ADD HL, BC
A374 004874  LD C, (HL)
A375 004875  PUSH BC
A376 004876  LD A, C
A377 004877  LD B, 02
A378 004878  CP 0A
A379 004879  JNR Z, A3F8
A380 004880  DEC B
A381 004881  CP 04
A382 004882  JNR NC, A401
A383 004883  LD A, 20
A384 004884  RST 18
A385 004885  DJNZ A3FC
A386 004886  POP BC
A387 004887  CALL 0ACD
A388 004888  POP HL
A389 004889  POP BC
A390 004890  LD DE, 0010
A391 004891  ADD HL, DE
A392 004892  DJNZ A30D
A393 004893  JR A30F
A394 004894  LD DE, 0010
A395 004895  ADD HL, DE
A396 004896  RET

```

SALTO AL VISCO

CONVIR 3.2.20.8

DISK ERROR

PUNTO POR CLAVE DISCO

0D06 = CLAVE TECLADO  
5BEA = CLAVE DISCO

```

LD A, (DE)
CP (HL)
RET NZ
INC DE
INC HL
DJNZ
RET

```

TITULO

FICHEROS

OP BORRADO S

A3B1 - 21593F - LD HL, "FICHEROS"

DF - RST 18

3AE45B - LD A, (5BE4)

21F45B - LD HL, 5BF4

96 - SUB (HL)

E5 - PUSH HL

CDBA3E - CALL 3EB4 - IMPRIME N°

21633F - LD HL, "BORRADO S"

DF - RST 18

E1 - POP HL

4E - LD C, (HL)

CDBB3E - CALL 3EB8 - IMPRIME N°

DEL TITULO

TITULO

NOMBRE

IMPRIME OB

FILE(S)

DEL. FILE(S)

PRINT "OB"

PRINT "A"

PRINT " "

"NOMBRE [B]"

PARA LOS ESPACIOS PORQUE LO PUEDE LEER SIN PROBLEMAS

ESPACIO

3E21 C9 RET - BYTE DE POR

3E70 C5 PUSH BC REFINA POR

D7 DIF 10H LA RUTAS

C1 POP BC AMERIZ

77 LD A, 3

FE02 CP 0E

C8 RET Z

3E20 LD A, 20H

D7 DIF 10H

3E70 LD A, 10H

V7 RET Z

C9 RET

AD1 OR A

B RET Z

CF C6 41 IMPRIME 106

V7 B.C.V

C9

3ED7 CD FF 3C

C3 29 03

1. PUNTO AL...  
2. PUNTO AL...  
3. PUNTO AL...

```

A4114 00000000  PUSH HL
A4115 00000000  PUSH BC
A4116 00000000  LD BC, A400
A4117 00000000  ADD HL, BC
A4118 00000000  LD R, H
A4119 00000000  OR R, R
A4120 00000000  JR NZ, A421
A4121 00000000  POP BC
A4122 00000000  POP HL
A4200 00000000  RET
A4201 00000000  LD HL, 5000
A4202 00000000  INC (HL)
A4203 00000000  CALL 0320
A4204 00000000  POP BC
A4205 00000000  POP HL
A4206 00000000  LD HL, 5500
A4207 00000000  RET
A4208 00000000  CALL 0B00
A4209 00000000  CALL 0B00
A4210 00000000  CALL 0AD2
A4211 00000000  LD R, C
A4212 00000000  CP B
A4213 00000000  JP NZ, 0A50
A4214 00000000  LD HL, (DE)
A4215 00000000  AND DF
A4216 00000000  SBC A, 41
A4217 00000000  JP C, 0A50
A4218 00000000  CP 04
A4219 00000000  JP NC, 0A50
A4220 00000000  LD (0019), A
A4221 00000000  CALL 00A9
A4222 00000000  JP 015E
A4223 00000000  CALL 0A5E
A4224 00000000  CALL 0A5E
A4225 00000000  CALL 0A5E
A4226 00000000  CALL 0A5E
A4227 00000000  LD R, (0CF6)
A4228 00000000  LD (0CF8), R
A4229 00000000  JP NZ, 0321
A4230 00000000  PUSH BC
A4231 00000000  CALL 0512
A4232 00000000  CALL 0A16
A4233 00000000  PUSH AF
A4234 00000000  LD R, (0CF8)
A4235 00000000  LD HL, 0CF8
A4236 00000000  CP (HL)
A4237 00000000  JP NZ, 0A50
A4238 00000000  CALL 034D → ERROR DISC
A4239 00000000  POP AF
A4240 00000000  JP NZ, 09AE
A4241 00000000  POP BC
A4242 00000000  CALL 0519
A4243 00000000  JP 001E
A4244 00000000  LD R, (5010)
A4245 00000000  OR R, R
A4246 00000000  RET
A4247 00000000  LD B, 43
A4248 00000000  LD R, (5CD6)
A4249 00000000  OR R, R
A4250 00000000  JR NZ, A4AA
A4251 00000000  CALL 0487
A4252 00000000  JR NZ, A4AA
A4253 00000000  CALL 09AE
A4254 00000000  CP AF
A4255 00000000  LD R, 43
A4256 00000000  JR NZ, A4AA
A4257 00000000  CP R, 44
A4258 00000000  LD B, 44
A4259 00000000  JR NZ, A4AA
A4260 00000000  LD B, 42
A4261 00000000  LD HL, 5CE5
A4262 00000000  LD (HL), B
A4263 00000000  RET

```

```

CALL 090000
CALL 090000
CALL 094000
CALL 0D0000 →
JP NZ, 0321
PUSH BC
CALL 09348
LD A, (5BE4)
POP BC
INC C
CP C
JR NZ, R4CF
DEC A
LD A, (5BE4), A
XOR A, A
PUSH H
JR NZ, R4D6
LD HL, 5BF4
INC (HL)
PUSH BC
CALL 090000
POP HL
DEC C
CALL 09012
POP HL
JP NZ, 04E5
LD A, 01
LD (5CDD), A
PUSH AF
CALL 09000
POP AF
JP NZ, 015E
CALL 0348
LD HL, (5CEB)
LD (5BE1), HL
LD DE, (5CE5)
LD HL, (5BE5)
LD D, 00
ADD HL, DE
LD (5BE5), HL
NR 3D1A →
CALL 09012
LD A, (5CDD)
CP 01
RET
XOR A
PUSH BC
CALL 065B
POP BC
RET
LD A, FF
JR A513
LD HL, (5C61), WORKSP
LD (5CCF), HL
LD BC, 1000
JP 0B64
LD (5CD7), HL
LD (5CDB), HL
LD DE, (5CEA)
LD HL, (5CD9)
LD D, 00
ADD HL, DE
LD (5CD9), HL
RET
CALL 0A96
CALL 051D
CALL 034D → ERROR D110
LD A, (5BF4)
OR A, A
JP NZ, 015E
LD HL, 0000
LD (5CD9), HL
LD C, FF
INC C
CALL 0609
JR NZ, A555
LD A, C
LD (5CD4), A
LD HL, (5CEB)
LD (5CD5), HL
CALL 09029
INC C
CALL 0509
JR NZ, A563
CP 00
JR NZ, A56A
LD A, (5CD4)
LD C, A
INC C
CALL 0509
CP 00
JR NZ, A5E6
XOR A, A
LD (5CDD), A
CALL 09000
CALL 09029
JR A578
LD A, (5CEA)
LD (5CD3), A
LD (5CD1), A
LD HL, (5CEB)
LD (5CD6), HL
PUSH BC
CALL 051F

```



```

A59D C1 POP BC
A59E 2AF45C LD HL, (SCF4)
A5A1 22D055C LD (SCD5), HL
A5A4 22E055C LD (SCEB), HL
A5A7 AF XOR A
A5A8 32E05C LD (SCEA), A
A5AB 3AD05C LD A, (SCDD)
A5AE F5 PUSH AF
A5AF 3E01 LD A, 01
A5B1 32D05C LD (SCDD), A
A5B4 CD9008 CALL 0890
A5B7 F1 POP AF
A5B8 32D05C LD (SCDD), A
A5BB 3AD45C LD A, (SCD4)
A5BE 4F LD C, A
A5BF 2AD05C LD HL, (SCDE)
A5C2 22E055C LD (SCEB), HL
A5C5 3AD15C LD A, (SCD1)
A5C8 32E05C LD (SCEA), A
A5CB CD9008 CALL 0890
A5CE 3AD45C LD A, (SCD4)
A5D1 3C INC A
A5D2 4F LD C, A
A5D3 CD1205 CALL 0512
A5D6 2AD055C LD HL, (SCD5)
A5D9 22E055C LD (SCEB), HL
A5DC CD9008 CALL 0890
A5DF 3AD45C LD A, (SCD4)
A5E2 4F LD C, A
A5E3 C35505 JP 0555

A5E6 2ACF5C LD HL, (SCCF)
A5E9 010310 LD BC, 1000
A5EC CD7008 CALL 0870
A5EF CD4803 CALL 0348
A5F2 2AE55B LD HL, (5BE5)
A5F5 ED58D95C LD DE, (SCD8)
A5F9 19 ADD HL, DE
A5FA 22E55B LD (5BE5), HL
A5FD 3AE458 LD A, (5BE4)
A600 217458 LD HL, 5BF4
A603 96 SUB (HL)
A604 32E45B LD (5BE4), A
A607 3800 LD (HL), 00
A609 2AD055C LD HL, (SCD5)
A60C 22E15B LD (5BE1), HL
A60F F5 PUSH AF
A610 CD9308 CALL 0893
A613 F1 POP AF
A614 4F LD C, A
A615 CD1205 CALL 0512
A618 AF XOR A
A619 32D05C LD (SCDD), A
A61C C38104 JP 0481
A61F 3AD35C LD A, (SCD3)
A622 B7 OR A
A623 C8 RET Z
A624 D810 SUB 10
A626 3025 JR NC, A653
A628 3AD35C LD A, (SCD3)
A62B 47 LD B, A
A62C AF XOR A
A62D 32D35C LD (SCD3), A
A630 C5 PUSH BC
A631 2ACF5C LD HL, (SCCF)
A634 E5 PUSH HL
A636 ED58055C LD DE, (SCD5)
A639 CD8008 CALL 0880
A63C 2AF45C LD HL, (SCF4)
A63F 22D055C LD (SCD5), HL
A642 E1 POP HL
A643 C1 POP BC
A644 ED58D75C LD DE, (SCD7)
A648 CD9D05 CALL 089D
A64B 2AF45C LD HL, (SCF4)
A64E 22D75C LD (SCD7), HL
A651 1800 JR A61F
A653 32D35C LD (SCD3), A
A656 0810 LD B, 10
A659 AF XOR A
A65B 1805 JR A630
A65E F5 PUSH AF
A660 21005C LD HL, 5000
A663 3800 LD (HL), 00
A666 79 LD A, C
A669 D810 SUB 10
A66C 3803 JR C, A669
A66F 34 INC (HL)
A672 18F2 JR A662
A675 0810 ADD A, 10
A678 4F LD C, A
A67B C5 PUSH BC
A67E CD2003 CALL 0320
A681 C1 POP BC
A684 F1 POP AF
A687 CD0A0A CALL 0A0A
A68A 11D05C LD DE, SCDD
A68D 011000 LD BC, 0010
A690 B7 OR A
A693 2801 JR Z, A67F
A696 EB LD DE, HL
A699 ED03 LDIR
A6A2 C9 RET

```

```

A6800 C000006 CALL 06C02
A6801 C000006 CALL 06998
A6802 C000006 CALL 0A986
A6803 3E777 LD A, FF
A6804 321050 LD (5D10), A
A6805 3A9E50 LD A, (5CE5)
A6806 77777 CP 42
A6807 C000006 JP Z, 06D9
A6808 C38E01 JP 015E

A6900 C000706 CALL 06C07
A6901 C00060A CALL 0A998
A6902 C000208 CALL 06F22
A6903 C030407 JP 0724
A6904 C00070B CALL 0A987
A6905 C00060A CALL 0A98E
A6906 FE00 CP 00
A6907 2A555C LD HL, (5C5D)
A6908 2B DEC HL
A6909 22555C LD (5C5D), HL
A6910 C3 RET Z
A6911 321050 LD (5D10), A
A6912 3A01 LD A, 01
A6913 3A055C LD (5C05), A
A6914 C00020B CALL 0B20
A6915 AF XOR A
A6916 321050 LD (5D10), A
A6917 C3 RET

A6C00 C000308 CALL 0B02
A6C01 C000704 CALL 0487
A6C02 C040508 CALL NZ, 0B06
A6C03 C00060A CALL 0A98E
A6C04 77777 CP AF
A6C05 C0001706 CALL Z, 06A7
A6C06 FE4 CP 04
A6C07 F5 PUSH AF
A6C08 C000C04 CALL 048C
A6C09 F1 POP AF
A6C10 C000609 CALL Z, 095E
A6C11 C00060A CALL 0A998
A6C12 C00030D CALL 3D88
A6C13 C000103 JP NZ, 0321
A6C14 C000103 CALL 0512
A6C15 C000103 CALL 3DF8
A6C16 C3 RET

A6E00 3A055C LD A, (5C05)
A6E01 B7 OR A
A6E02 2A555C LD HL, (5CE5)
A6E03 2B JR Z, A6FE
A6E04 2A055C LD HL, (5C09)
A6E05 2B LD DE, (5CEB)
A6E06 FE03 CP 03
A6E07 3A055C LD A, (5CEA)
A6E08 D5 PUSH DE
A6E09 2B07 JR NZ, A711
A6E10 2A055C LD DE, (5C0B)
A6E11 2B05 CALL 0B05
A6E12 F5 PUSH AF
A6E13 3A055C LD A, (5CE5)
A6E14 FE4 CP 42
A6E15 F5 PUSH AF
A6E16 2B07 CALL Z, 07A5
A6E17 F1 POP AF
A6E18 FE44 CP 44
A6E19 C000707 CALL Z, 07D7
A6E20 F1 POP AF
A6E21 D1 POP DE
A6E22 C3 RET

A7000 47 LD B, A
A7001 C000704 CALL 0487
A7002 2B07 JR Z, A731
A7003 F5 PUSH AF
A7004 C01208 CALL 0812
A7005 F1 POP AF
A7006 FEFF CP FF
A7007 F5 PUSH AF
A7008 C000008 CALL Z, 0B8D
A7009 3A055C LD A, (5C05)
A7010 FE03 CP 03
A7011 C00003F CALL Z, 3F0D
A7012 F1 POP AF
A7013 C49008 CALL NZ, 0B9D
A7014 2A555C LD HL, (5C59)
A7015 2B DEC HL
A7016 3B80 LD (HL), 80
A7017 C3 RET

A7400 3E777 LD A, FF
A7401 1802 JR A74E
A7402 3E777 LD A, EE
A7403 321050 LD (5D10), A
A7404 C38E01 JP 0655

```

CODE  
DATA

SC

"B"

"D"

"B"

"D"

```

A754 CDC706 CALL 06C7
A757 CD950A CALL 0A95
A75A 3AE55C LD A, (5CE5)
A75D FE42 CP 42 → "8"
A75F C2600A JP NZ, 0A50
A762 ED4BE65C LD BC, (5CE6)
A766 05 PUSH BC
A767 03 INC BC
A768 213000 LD HL, 0030
A76B CDEE0A CALL 0ABE
A76E 3680 LD (HL), 80
A770 EB EX DE, HL
A771 D1 POP DE
A772 E5 PUSH HL
A773 ED58E55C LD DE, (5CEB)
A777 3AE55C LD A, (5CEA)
A77A 47 E A
A77B CDC206 CALL 06C2
A77E 73 LD A, B
A77F CD2407 CALL 0724
A782 E1 POP HL
A783 22025D LD (5D02), HL
A786 ED58E55C LD DE, (5C53)
A78A 21D208 LD HL, 08D2
A78D CD750B CALL 0B75
A790 C38B06 JP 068B
A793 EB EX DE, HL
A794 37 SCF
A795 ED52 SBC HL, DE
A797 D3 RET C
A798 110A00 LD DE, 000A
A79B 19 ADD HL, DE
A79C 44 LD B, H
A79D 4D LD C, L
A79E 21051F LD HL, 1F05
A7A1 CDEE0A CALL 0ABE
A7A4 09 RET
A7A5 ED58E55C LD DE, (5C53)
A7A9 2AE55C LD HL, (5C59)
A7AC 2B DEC HL
A7AD E5 PUSH HL
A7AE DE PUSH DE
A7AF ED52 SBC HL, DE
A7B1 ED58E65C LD DE, (5CE6)
A7B5 D5 PUSH DE
A7B8 CD9307 CALL 0793
A7B9 C1 POP BC
A7BA D1 POP DE
A7BB E1 POP HL
A7BC 05 PUSH BC
A7BD 22025D LD (5D02), HL
A7C0 21E519 LD HL, 19E5
A7C3 CD750B CALL 0B75
A7C6 C1 POP BC
A7C7 CD850B CALL 0B85
A7CA 23 INC HL
A7CB ED4BE65C LD BC, (5CE8)
A7CF 09 ADD HL, BC
A7D0 22455C LD (5C4B), HL
A7D3 2AE55C LD HL, (5C53)
A7D6 09 RET
A7D7 ED58E65C LD DE, (5CE8)
A7DB 2AD55C LD HL, (5CDB)
A7DE E5 PUSH HL
A7DF CD9307 CALL 0793
A7E2 E1 POP HL
A7E3 7C LD A, H
A7E4 B5 OR L
A7E5 D810 JR Z, A7F7
A7E7 2AD75C LD HL, (5CD7)
A7EA 2B DEC HL
A7EB 2B DEC HL
A7EC 2B DEC HL
A7ED ED4BD55C LD BC, (5CDB)
A7F1 03 INC BC
A7F2 03 INC BC
A7F3 03 INC BC
A7F4 CD7D0B CALL 0B7D
A7F7 2AE55C LD HL, (5C59)
A7FA 2B DEC HL
A7FB ED4BE65C LD BC, (5CE8)
A7FF 05 PUSH BC
A800 03 INC BC
A801 03 INC BC
A802 03 INC BC
A803 CD850B CALL 0B85
A806 23 INC HL
A807 3AD25C LD A, (5CD2)
A80A 77 LD (HL), A
A80B 23 INC HL
A80C D1 POP DE
A80D 73 LD (HL), E
A80E 23 INC HL
A80F 72 LD (HL), D
A810 23 INC HL
A811 09 RET

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A012 3A095C LD A, (5CD9)
A013 4470 LD B,C,B
A014 7700 LD B,A,C
A015 0800 CP B,A
A016 0821 JR CC,A830
A017 7700 LD A,B
A018 0800 OR A,B
A019 0A60 JP NZ,0A60
A020 0800 DEC B
A021 0836 JR NZ,A836
A022 0800 PUSH DE
A023 1104 LD DE,5CC4
A024 7700 LD HL,(5CF8)
A025 0800 ADD HL,DE
A026 0800 POP DE
A027 0800 LD A,(HL)
A028 0800 INC A
A029 0800 CP A
A030 0800 JR NZ,A834
A031 0800 LD E,00
A032 0800 INC D
A033 0800 DJNZ A82D
A034 0800 LD B,01
A035 0800 LD HL,(5CD7)
A036 0800 RET
A037 0800 LD HL,3FAE -
A038 0800 LD A,05
A039 0800 JP 09A8
A040 0800 CALL 0D38
A041 0800 JP NZ,09AE
A042 0800 CALL 0348
A043 0800 LD A,(5BE4)
A044 0800 CP 00
A045 0800 JP NZ,09A3
A046 0800 RET
A047 0800 CALL 06C2
A048 0800 LD HL,0001
A049 0800 LD (5CD1),HL
A050 0800 CALL 0800
A051 0800 CALL 0AAE
A052 0800 CP AF
A053 0800 JR NZ,A8EB
A054 0800 CP AF
A055 0800 JR NZ,A87E
A056 0800 CALL 0848
A057 0800 CALL 0A96
A058 0800 LD HL,(5CDE)
A059 0800 LD (5CD1),HL
A060 0800 LD HL,5CE5
A061 0800 LD (58AE),HL
A062 0800 CP AF
A063 0800 JR NZ,A880
A064 0800 LD HL,4000
A065 0800 LD (5CD7),HL
A066 0800 LD HL,5E00
A067 0800 LD (5CD9),HL
A068 0800 JR A88F
A069 0800 CALL 0A96
A070 0800 CALL 0AAE
A071 0800 LD HL,5CE5
A072 0800 CP E4
A073 0800 JR NZ,A8AF
A074 0800 CP 00
A075 0800 JP NZ,0A60
A076 0800 LD (HL),42
A077 0800 CALL 0844
A078 0800 CALL 0858
A079 0800 CALL 0858
A080 0800 JR A8C9

```

REC. NO. 11

CODE  
LINE

SCREEN

DATA

```

A8AF 3E44 LD (HL),44
A8B1 CD4408 CALL 0844
A8B4 CD7909 CALL 0979
A8B7 3040 JR NC,A8C9
A8B9 3818 JR C,A8D6
A8BB CD060B CALL 080B
A8BE CD950A CALL 0A95
A8C1 3E43 LD A,43
A8C3 32E55C LD (SCE5),A
A8C6 CD4408 CALL 0844
A8C9 2AD75C LD HL,(SCD7)
A8CC 22E65C LD (SCE6),HL
A8CF EB EX DE,HL
A8D0 2AD95C LD HL,(SCD9)
A8D3 B7 OR A
A8D4 ED52 SBC HL,DE
A8D6 DA600A JP C,0A60
A8D9 7D LD A,L
A8DA B7 OR A
A8DB 2801 JR Z,A8DE
A8DD 24 INC H
A8DE 7C LD A,H
A8DF 32EA5C LD (SCEA),A
A8E2 5F LD E,A
A8E3 1800 LD D,00
A8E5 2AE55B LD HL,(SBE5)
A8E8 ED52 SBC HL,DE
A8EA DA9309 JP C,09A3
A8ED EB PUSH HL
A8EF 2A595C LD HL,(SC59)
A8F1 36AA LD (HL),AA
A8F3 23 INC HL
A8F4 ED5B015C LD DE,(SCD1)
A8F8 73 LD (HL),E
A8F9 23 INC HL
A8FA 72 LD (HL),D
A8FB 2AD85C LD HL,(SCD8)
A8FE 22E85C LD (SCE8),HL
A901 2AE15B LD HL,(SBE1)
A904 22E65C LD (SCE6),HL
A907 EB PUSH HL
A908 CDFACE CALL 3EFA →
A90B E1 POP HL
A90C EB EX DE,HL
A90D 2AE65C LD HL,(SCE6)
A910 3AEA5C LD A,(SCEA)
A913 47 LD B,A
A914 CD9D0B CALL 0B9D
A917 2AF45C LD HL,(SCF4)
A91A EB PUSH HL
A91B CD4803 CALL 0348
A91E E1 POP HL
A91F 22E15B LD (SBE1),HL
A922 E1 POP HL
A923 22E55B LD (SBE5),HL
A926 21E45B LD HL,SBE4
A929 34 INC (HL)
A92A EB PUSH HL
A92B CD930B CALL 0B93
A92E E1 POP HL
A92F 4E LD C,(HL)
A930 00 DEC C
A931 3AE55C LD A,(SCE5)
A934 7E42 CP 42 → "B"
A936 CD3C09 CALL Z,093C
A939 C38104 JP 0481
A93C 2A595C LD HL,(SC59)
A93F ED5B535C LD DE,(SC53)
A943 37 SCF
A944 ED52 SBC HL,DE
A946 22E65C LD (SCE6),HL
A949 2A4B5C LD HL,(SC4B)
A94C ED52 SBC HL,DE
A94E 22E65C LD (SCE6),HL
A951 C9 RET
A952 2A4B5C LD HL,(SC4B)
A955 ED5B535C LD DE,(SC53)
A959 ED52 SBC HL,DE
A95B 2AD85C LD (SCD8),HL
A95E 2A535C LD HL,(SC53)
A961 2AD75C LD (SCD7),HL
A964 2A595C LD HL,(SC59)
A967 23 INC HL
A968 23 INC HL
A969 23 INC HL
A96A 22D95C LD (SCD9),HL
A96D C9 RET
A96E CD7909 CALL 0979
A971 D0 RET NC
A972 210000 LD HL,0000
A975 22DB5C LD (SCDB),HL
A978 C5 SET

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AA0700 CDEF0B CALL 0B6F
AA0701 CDC00A CALL 0A03
AA0702 CBF9 SET 7,C
AA0703 799D LD A,C
AA0704 32D25C LD (SCD2),A
AA0705 799D JR NZ,A989
AA0706 0C74 SCF
AA0707 0C74 RET
AA0708 0C74 FC JR NZ,A987
AA0709 0C74 INC HL
AA0710 0C74 LD E,(HL)
AA0711 0C74 INC HL
AA0712 0C74 LD D,(HL)
AA0713 0C74 INC HL
AA0714 0C74 LD (SCD7),HL
AA0715 0C74 LD (SCD8),DE
AA0716 0C74 ADD HL,DE
AA0717 0C74 LD (SCD9),HL
AA0718 0C74 CALL 0B6F
AA0719 0C74 CP 29
AA0720 0C74 JR NZ,A989
AA0721 0C74 RET
AA0722 0C74 LD HL,3F70 NO SPACE
AA0723 0C74 LD A,03
AA0724 0C74 CALL 0316
AA0725 0C74 JP 015F
AA0726 0C74 LD HL,3F7B FILE EXISTS
AA0727 0C74 LD A,02
AA0728 0C74 JR A989
AA0729 0C74 LD HL,SCDD
AA0730 0C74 LD B,03
AA0731 0C74 LD (HL),20
AA0732 0C74 INC HL
AA0733 0C74 DJNZ A9BA
AA0734 0C74 CALL 0A02
AA0735 0C74 LD A,B
AA0736 0C74 OR C
AA0737 0C74 JP NZ,0A60
AA0738 0C74 EX DE,HL
AA0739 0C74 CALL 090E
AA0740 0C74 LD A,C
AA0741 0C74 CP 09
AA0742 0C74 JR C,A9D2
AA0743 0C74 LD C,03
AA0744 0C74 LD A,(HL)
AA0745 0C74 CP 20
AA0746 0C74 JP C,0A60
AA0747 0C74 LD DE,SCDD
AA0748 0C74 LDIR
AA0749 0C74 RET
AA0750 0C74 INC HL
AA0751 0C74 LD A,(HL)
AA0752 0C74 CP 3A
AA0753 0C74 JR NZ,A9FE
AA0754 0C74 DEC HL
AA0755 0C74 LD A,(HL)
AA0756 0C74 AND DF 1101 1111
AA0757 0C74 SBC A,41
AA0758 0C74 JP C,0A60
AA0759 0C74 CP 04
AA0760 0C74 JP NC,0A60
AA0761 0C74 PUSH BC
AA0762 0C74 PUSH HL
AA0763 0C74 CALL 30A9
AA0764 0C74 POP HL
AA0765 0C74 POP BC
AA0766 0C74 DEC BC
AA0767 0C74 DEC BC
AA0768 0C74 INC HL
AA0769 0C74 INC HL
AA0770 0C74 RET
AA0771 0C74 DEC HL
AA0772 0C74 LD A,(5D19)
AA0773 0C74 PUSH BC
AA0774 0C74 PUSH HL
AA0775 0C74 CALL 30A9
AA0776 0C74 POP HL
AA0777 0C74 POP BC
AA0778 0C74 RET
AA0800 0C74 LD L,C
AA0801 0C74 LD H,00
AA0802 0C74 ADD HL,HL
AA0803 0C74 ADD HL,HL
AA0804 0C74 ADD HL,HL
AA0805 0C74 LD BC,5B00
AA0806 0C74 ADD HL,BC
AA0807 0C74 RET

```

IMPRESSION  
RECL

NO SPACE

FILE EXISTS

1101 1111

```

AA16 CDB509 CALL 09B5
AA19 CD2903 CALL 0329
AA1C 0E580 LD B,80
AA1E 0E08 LD C,00
AA20 C5 PUSH BC
AA21 CD0A0A CALL 0A0A
AA24 CD1404 CALL 0414
AA27 C1 POP BC
AA28 C5 PUSH BC
AA29 79 LD A,C
AA2A FE10 CP 10
AA2C 2005 JR NZ,AA33
AA2E C1 POP BC
AA2F 0E08 LD C,00
AA31 18ED JR AA20
AA33 11005C LD DE,5CDD
AA36 0E09 LD B,09
AA38 AF XOR A
AA39 BE CP (HL)
AA3A 2003 JR NZ,AA3F
AA3C C1 POP BC
AA3D 1809 JR AA48
AA3F CD0E30 CALL 0E30
AA42 C1 POP BC
AA43 2005 JR Z,AA4B
AA46 0C INC C
AA48 10D8 DJNZ AA20
AA4B F8FF OR FF
AA4A C9 RET
AA4B 0E80 LD A,80
AA4D 90 SUB B
AA4E 4F LD C,A
AA4F AF XOR A
AA50 C9 RET
AA51 CD213D CALL 2D21
AA54 FDCB019E RES 3,(IY+01)
AA58 CD0D01 CALL 0D01
AA5B ED7B1C5D LD SP,(SD1C)
AA5F C9 RET
AA60 FDC5007E BIT 7,(IY+00)
AA64 2005 JR Z,AA6B
AA66 0E08 LD A,08
AA68 323A5C LD (5C3A),A
AA6B 0C INC A
AA6C 21673F LD HL,3F67
AA6F CD1503 CALL 1503
AA72 C35E01 JP 015E
AA75 CDC208 CALL 0208
AA78 CD9B06 CALL 0B06
AA7B CD9609 CALL 0609
AA7E 2A035C LD HL,(5C03)
AA81 3A055C LD A,(5C05)
AA84 7E42 CP 42
AA86 C9D900 JP Z,00D9
AA89 85 PUSH HL
AA8B 215E01 LD HL,015E
AA8D 85 PUSH HL
AA8E C3903C JP 3C90
AA91 FDCB017E BIT 7,(IY+01)
AA95 C9 RET
AA96 CD910A CALL 0A91
AA99 C0 RET NZ
AA9A E1 POP HL
AA9B C9 RET
AA9C CD5F08 CALL 0F08
AA9F CDE10A CALL 0E10
AAA2 18ED JR AA91
AAA4 AF XOR A
AAA5 210116 LD HL,1601
AAA8 1814 JR AA5E
AAA9 3E02 LD A,02
AAAC 18F7 JR AA85
AAAE 211800 LD HL,0018
AAB1 1808 JR AA8E
AAB3 CD0A0A CALL 0A0A
AAB5 212C0F LD HL,0F2C
AAB9 1803 JR AA8E
AABB 21550D LD HL,0D55
AABE 85 PUSH HL
AABF CD903C CALL 3C90
AAC2 C9 RET
AAC3 215228 LD HL,2828
AAC6 18F6 JR AA8E
AAC8 215E0D LD HL,0D5E
AACB 18F1 JR AA8E
AACD 21181A LD HL,1A18
AAD0 18EC JR AA8E
AAD2 21F12B LD HL,2BF1
AAD5 18E7 JR AA8E
AAD7 21991E LD HL,1E99
AAD9 18E2 JR AA8E
AAC0 218C10 LD HL,108C
AADF 18DD JR AA8E
AAE1 218210 LD HL,1082
AAE4 18D8 JR AA8E
AAE6 2A115D LD HL,(SD11)
AAE9 23 INC HL
AAEA 22505C LD (5C5D),HL
AAED C9 RET

```

\* ERROR \*

CANAL "0"  
CANAL "1"

CANAL

CLS  
CONTROL PUERTOS

LOOK-VARS

CLS-LAW

LIVE NUMBER

SEPARA NÚM Y STRING

FIND INTEGERS

EVALUA EXPRESION

EVALUA - NEXT

SALTOS AL SISTEMA

```

ABEE CD000B CALL 0B00
ABF1 CD0E0A CALL 0B0E
ABF4 FE2C CP 2C -> ", "
ABF6 C2800A JP NZ, 0A60
ABF9 CD8F0B CALL 0B6F
ABFC CD0C0A CALL 0BDC
ABFF C9 RET
AB00 CDE80A CALL 0A85
AB03 CD0C0A JP 0ADC
AB06 CD0E0A CALL 0A8E
AB09 FEAF CP AF -> "OLE"
AB0E C0 RET NZ
AB0C CD9C0A CALL 0A9C
AB0F 2807 JR Z, AB18
AB11 CD070A CALL 0AD7
AB14 ED43D75C LD (5CD7), BC
AB16 CD0E0A CALL 0A8E
AB1B FE2C CP 2C -> ", "
AB1D C2800A JP NZ, 0A60
AB20 CD9C0A CALL 0A9C
AB23 2813 JR Z, AB38
AB26 CD070A CALL 0AD7
AB28 CD8704 CALL 0487
AB2B ED43D95C LD (5CD9), BC
AB2F 2807 JR NZ, AB38
AB31 2AD75C LD HL, (5CD7)
AB34 03 ADD HL, BC
AB35 22D95C LD (5CD9), HL
AB38 CD0E0A CALL 0A8E
AB3B FE2C CP 2C -> ", "
AB3D 2809 JR Z, AB48
AB3F FE0D CP 0D
AB41 C2800A JP NZ, 0A60
AB44 CD0E0A CALL 0A8E
AB47 C9 RET
AB48 CD9C0A CALL 0A9C
AB4B C8 RET Z
AB4C CD070A CALL 0AD7
AB4F ED43D85C LD (5CD8), BC
AB53 3E03 LD A, 03
AB55 32D85C LD (5CD8), A
AB58 C9 RET
AB59 2A115D LD HL, (5D11)
AB5C 22025D LD (5D02), HL -> REMOVE FLOAT POINT
AB5F 21A711 LD HL, 11A7
AB62 1811 JR AB75
AB64 2A815D LD HL, (5C81)
AB67 22025D LD (5D02), HL
AB6A 213000 LD HL, 0030 -> MAKE BC SPACES
AB6D 1806 JR AB75
AB6F 22025D LD (5D02), HL
AB72 212000 LD HL, 0020 -> COLLECT NEXT CHAR
AB75 E5 PUSH HL
AB76 2A025D LD HL, (5D02)
AB79 CD903C CALL 3C90 ->
AB7C C9 RET
AB7D 22025D LD (5D02), HL
AB80 21E819 LD HL, 19E8 -> RECLAIMING
AB83 18F0 JR AB75
AB86 22025D LD (5D02), HL
AB88 215518 LD HL, 1855 -> MAKE ROOM
AB8B 18E8 JR AB75
AB8D AF XOR A
AB8E 180F JR AB9F
AB90 CD1905 CALL 0519
AB93 ED58F45C LD DE, (5CF4)
AB97 18 DEC DE
AB98 0601 LD B, 01
AB9A 21005B LD HL, 5B00
AB9D 3EFF LD A, FF
AB9F 32CE5C LD (5CCE), A
ABA2 ED53F45C LD (5CF4), DE
ABA6 AF XOR A
ABA7 80 OR B
ABA8 C8 RET Z
ABA9 C5 PUSH BC
ABAA E5 PUSH HL
ABAB CD2E3E CALL 3E2E
ABAE 3AF45C LD A, (5CF4)
ABB1 CD2A3E CALL 3E2A
ABB4 3AF55C LD A, (5CF5)
ABB7 CD0CB0D CALL 30CB
ABBA 3ACE5C LD A, (5CCE)
ABBD B7 OR A
ABBE 75 PUSH AF
ABBF DC383E CALL Z, 3E38
ABC2 F1 POP AF
ABC3 C4323E CALL NZ, 3E32
ABC6 E1 POP HL
ABC7 110001 LD DE, 0100
ABCA 19 ADD HL, DE
ABC8 E5 PUSH HL
ABCC 11045C LD DE, 50C4
ABCF 2AF65C LD HL, (5CF6)
ABD2 19 ADD HL, DE
ABD3 7E LD A, (HL)
ABD4 21F45C LD HL, 5CF4
ABD7 34 INC (HL)
ABD8 BE CP (HL)
ABDB 2806 JR NZ, ABE1
ABDE 3603 LD (HL), 00
ABDD 21F55C LD HL, 5CF5
ABE0 34 INC (HL)
ABE1 E1 POP HL
ABE2 C1 POP BC
ABE3 10C4 DJNZ AB85
ABE5 C9 RET

```



AB06	00000000	PUSH	HL
AB07	00000000	LD	H,A
AB08	00000000	LD	L,00
AB09	00000000	PUSH	HL
AB0A	00000000	SEC	HL,DE
AB0B	00000000	POP	HL
AB0C	00000000	CALL	C,00F5
AB0D	00000000	LD	A,H
AB0E	00000000	POP	HL
AB0F	00000000	RET	C
AB10	00000000	LD	A,D
AB11	00000000	RET	
AB12	00000000	XOR	A
AB13	00000000	LD	(5CD6),A
AB14	00000000	SCF	
AB15	00000000	RET	
AB16	00000000		
AB17	00000000		
AB18	00000000		
AB19	00000000		
AB1A	00000000		
AB1B	00000000		
AB1C	00000000		
AB1D	00000000		
AB1E	00000000		
AB1F	00000000		

LIBRES

ENTRADA DESDE BASIC

3Cφφ

ENTRADA DESDE DISCO ESPANZO

IN CAT

```

HL000 038130 JP 3081 → PRESENZA CABECERA ETC
AC003 032930 JP 3029 → WHITE & ZEN:
AC006 03A930 JP 30A9
AC009 03600B JP 0E80
AC00C 039D0B JP 0E90
AC00F 2A105D LD HL, (5D10)
AC12 2B5 DEC HL
AC13 2B5 DEC HL
AC14 79 LD SP, HL
AC15 0DAA30 CALL 30AA
AC18 03600A JP 0E80
AC1B ED7E3D5C LD SP, (5C3D)
AC17 2A105D LD A, (5D10)
AC22 B7 OR A
AC23 CA781B JP Z, 1B78 → ROM
AC25 03CF12 JP 12CF → ROM
AC29 2A175D LD A, (5D17)
AC2C FEAR CP AA
AC2E C43830 CALL NZ, 3038
AC31 0DAA30 CALL 30AA
AC34 E5 PUSH HL
AC35 030E01 JP 010E
AC38 D8F7 IN A, (F7)
AC3A FE1E CP 1E
AC3C 2002 JR NZ, AC40
AC3E CA RST 8
AC3F 3121B5 LD SP, B521
AC42 5C LD E, H
AC43 017000 LD BC, 0070
AC46 CD5516 CALL 1655 → ROM MAKE ROOM
AC49 3E08 LD A, 08
AC4B 321E5D LD (5D1E), A
AC4E AF XOR A
AC4F 32185D LD (5D18), A
AC52 320F5D LD (5D0F), A
AC55 32195D LD (5D19), A
AC58 3EFF LD A, FF
AC5A 323A5C LD (5C3A), A
AC5D 32165D LD (5D16), A
AC60 21243F LD HL, 3F24
AC63 221F5D LD (5D1F), HL
AC66 21313F LD HL, 3F31
AC69 22215D LD (5D21), HL
AC6C 3E00 LD A, 00
AC6E 32235D LD (5D23), A
AC71 0DD230 CALL 30D2
AC74 3E00 LD A, 00
AC76 D31F OUT (1F), A → DEIVE & ETC SEL
AC78 C9 RET
AC79 3EFF LD A, FF
AC7B 32165D LD (5D16), A
AC7E 0DBE30 CALL 30BE
AC81 2A175D LD A, (5D17) → PRIMEA ENIL
AC84 FEAR CP AA
AC86 C43830 CALL NZ, 3038
AC89 0DAA30 CALL 30AA
AC8C E5 PUSH HL
AC8D 03C401 JP 01C4
AC8F 22025D LD (5D02), HL
AC93 ED53045D LD (5D04), DE } SCRATCH
AC97 D1 POP DE
AC98 F1 POP HL
AC99 D9 PUSH DE
AC9A 0DBE30 CALL 30BE
AC9D 11AD30 LD DE, 30AD
ACA0 D9 PUSH DE
ACA1 E5 PUSH HL
ACA2 ED58045D LD DE, (5D04) } SCRATCH
ACA6 2A025D LD HL, (5D02) } SCRATCH
ACA9 C9 RET
ACAB 21BE30 LD HL, 30BE
ACAD 79 DI
ACAE F9 PUSH AF
ACAF 0DD230 CALL 30D2
ACB2 2A165D LD A, (5D16)
ACB5 2B7F AND 7F
ACB7 32165D LD (5D16), A
ACBA D3FF OUT (FF), A → CENSA REGI: LATCH
ACBC F1 POP AF
ACBD C9 RET
ACBE F9 PUSH AF
ACBF 0DD230 CALL 30D2
ACC2 2A165D LD A, (5D16)
ACC5 F880 OR 80
ACC7 32165D LD (5D16), A
ACCA D3FF OUT (FF), A → MANTENE BLOQUEADO PAG CERO LATCH
ACCC 0DD230 CALL 30D2
ACCF F1 POP AF
ACD0 F9 EI
ACD1 C9 RET
ACD2 0DBE30 CALL 30BE
ACD5 D3FC OUT (FC), A → BIEST PERMISO DOS ACCESO CONTROLADO.
ACD7 C9 RET
ACD8 0DBE30 CALL 30BE
ACDB F880 OR 80
ACDD D3FC OUT (FC), A → BIEST NO PERMISO DOS
ACDF C9 RET
ACE0 2A485C LD A, (5C48)
ACE3 E638 AND 38 → 00111000
ACE5 0F RRCA
ACE6 0F RRCA
ACE7 0F RRCA
ACE8 C9 RET

```

TRIESADO

ROM MAKE ROOM

2002 JR NC  
CF ?  
31 ?  
→ 21B556 LD HL, 5C85

DEIVE & ETC SEL

PRIMEA ENIL

SCRATCH

SCRATCH

0111 1111 → SOFTWARE DISCO = 51

CENSA REGI: LATCH

MANTENE BLOQUEADO PAG CERO LATCH

BIEST PERMISO DOS ACCESO CONTROLADO.

BIEST NO PERMISO DOS

00111000

```

AC000 0000230  CALL 30D2
AC001 0000230  LD  A,FF
AC002 0000230  OUT (FF),A
AC003 0000230  RET
AC004 0000230  CALL 30E9
AC005 0000230  LDDR
AC006 0000230  JR  ACAD
AC007 0000230  CALL 30E9
AC008 0000230  LDIR
AC009 0000230  JR  ACAD
AC010 0000230  LD  A,00
AD001 0000230  PUSH HL
AD002 0000230  PUSH BC
AD003 0000230  CALL 3D09
AD004 0000230  POP  BC
AD005 0000230  POP  HL
AD006 0000230  RET
AD007 0000230  LD  HL,0010
AD008 0000230  JR  00BE
AD009 0000230  LD  A,(HL)
AD010 0000230  OR  A
AD011 0000230  RET  Z
AD012 0000230  AND 7F
AD013 0000230  RST 10
AD014 0000230  BIT 7,(HL)
AD015 0000230  RET  NZ
AD016 0000230  INC HL
AD017 0000230  JR  AD0F
AD018 0000230  CALL 00B8
AD019 0000230  JP  015F
AD020 0000230  LD  A,(SC0B)
AD021 0000230  CP  F4
AD022 0000230  RET  Z
AD023 0000230  LD  HL,5D18
AD024 0000230  OR  (HL)
AD025 0000230  LD  (HL),FF
AD026 0000230  RET  Z
AD027 0000230  LD  HL,50B6
AD028 0000230  LD  DE,5D28
AD029 0000230  LD  B,3A
AD030 0000230  LD  C,(HL)
AD031 0000230  LD  A,(DE)
AD032 0000230  LD  A,C
AD033 0000230  LD  (DE),A
AD034 0000230  INC HL
AD035 0000230  INC DE
AD036 0000230  DJNZ AD36
AD037 0000230  RET
AD038 0000230  LD  HL,(SC59)
AD039 0000230  LD  (HL),00
AD040 0000230  LD  (SC5B),HL
AD041 0000230  INC HL
AD042 0000230  LD  (HL),80
AD043 0000230  RET
AD044 0000230  LD  A,(5D0F)
AD045 0000230  OR  A
AD046 0000230  CALL Z,3D40
AD047 0000230  LD  HL,(SC59)
AD048 0000230  CALL 30FF
AD049 0000230  LD  A,(5D19)
AD050 0000230  ADD A,41
AD051 0000230  RST 10
AD052 0000230  LD  A,3E
AD053 0000230  RST 10
AD054 0000230  LD  HL,503A
AD055 0000230  LD  (HL),FF
AD056 0000230  CALL 00B3
AD057 0000230  CALL 00C8
AD058 0000230  RET
AD059 0000230  LD  A,(DE)
AD060 0000230  CP  (HL)
AD061 0000230  RET  NZ
AD062 0000230  INC DE
AD063 0000230  INC HL
AD064 0000230  DJNZ AD6E
AD065 0000230  RET
AD066 0000230  PUSH BC
AD067 0000230  LD  B,08
AD068 0000230  LD  A,(HL)
AD069 0000230  RST 10
AD070 0000230  INC HL
AD071 0000230  DJNZ AD79
AD072 0000230  LD  A,3C
AD073 0000230  RST 10
AD074 0000230  LD  A,(HL)
AD075 0000230  RST 10
AD076 0000230  LD  A,3E
AD077 0000230  RST 10
AD078 0000230  LD  A,3E
AD079 0000230  RST 10
AD080 0000230  POP  BC
AD081 0000230  RET
AD082 0000230  CALL 00E5
AD083 0000230  CALL 004D
AD084 0000230  JP  001E
AD085 0000230  LD  DE,SCFA
AD086 0000230  LD  HL,(SCF8)
AD087 0000230  ADD HL,DE
AD088 0000230  XOR  A
AD089 0000230  LD  (HL),A
AD090 0000230  LD  A,(5D1E)
AD091 0000230  OUT (1F),A
AD092 0000230  IN  A,(FF)
AD093 0000230  AND 80
AD094 0000230  JR  Z,AD9F
AD095 0000230  BET

```

3CFF

RST 10H

3D09

IMPRIME MESSAGE

IN CAT

IMPRIME TEXTO S/ HL

CANTIDAD DE CARACTERES ?

CD 118

COMPARA LA CLAVE

HL = 5B10

IMPRIME NUMBRE

IMPRIME :  
NUMBRE <B>

IN CAT

JN  
CAT

```

→ AD06 3A108D LD A,(5D19)
AD07 002A8D LD (SCF6),A →
AD08 21158D LD HL,5D16
AD09 4F LD C,A
AD0A 3E7C LD A,7C
AD0B B1 OR C
AD0C D3FF OUT (FF),A
AD0D 77 LD (HL),A
AD0E 11F8 LD DE,SCFA
AD0F 2A788C LD HL,(SCF6)
AD10 19788C ADD HL,DE
AD11 78 LD A,(HL)
AD12 D33F OUT (3F),A
AD13 3E9F LD A,9F
AD14 009F LD C,FF
AD15 009F DEC C
AD16 209FD JR NZ,ADC4 } TEMPORARY
AD17 3D DEC A
AD18 209F8 JR NZ,ADC2
AD19 C9 RET
AD20 4F LD C,A
AD21 D81F IN A,(1F)
AD22 E888 AND 88
AD23 3E00 LD (SCCD),A
AD24 E088 LD DE,(SCF6)
AD25 21A88C LD HL,SCFA
AD26 19788C ADD HL,DE
AD27 3D16 LD A,(5D16)
AD28 F67C OR 7C
AD29 3E16 LD (5D16),A
AD30 D37F OUT (FF),A
AD31 71 LD (HL),C
AD32 E9 PUSH HL
AD33 19C88C LD HL,SCC8
AD34 78 ADD HL,DE
AD35 78 LD A,(HL)
AD36 E1 POP HL
AD37 F817 CP 17
AD38 00183E CALL Z,3E18
AD39 F818 CP 18
AD40 00183E CALL Z,3E18
AD41 78 LD A,C
AD42 D37F OUT (7F),A
AD43 3A1E5D LD A,(5D1E)
AD44 F618 OR 18
AD45 D81F OUT (1F),A
AD46 3A008C LD A,(SCCD)
AD47 B7 OR A
AD48 2888 JR NZ,AE10
AD49 0988 LD B,02
AD50 3E88 LD A,E8
AD51 00003D CALL 3D00
AD52 19788C DJNZ AE09
AD53 00003D CALL 3D0F
AD54 3D18 LD A,18
AD55 00003D JP 3D02
AD56 43 LD B,A
AD57 78 LD A,C
AD58 B7 OR A
AD59 1F RRA
AD60 4F LD C,A
AD61 78 LD A,B
AD62 D3 RET NC
AD63 3A165D LD A,(5D16)
AD64 E888 AND 88
AD65 D3FF OUT (FF),A
AD66 3E165D LD (5D16),A
AD67 C9 RET
AD68 3E7F5C LD (SCFF),A
AD69 C9 RET
AD70 2E005D LD (5D00),HL
AD71 C9 RET
AE32 3E80 LD A,80
AE34 1802 JR AE38

```

```

AE36 3E69 LD A,80
AE38 32FE5C LD (SCFE),A
AE3B 160A LD D,0A
AE3D D5 PUSH DE
AE3E 3AFF5C LD A,(SCFF)
AE41 3C INC A
AE42 D35F OUT (SF),A
AE44 2A035D LD HL,(5000)
AE47 3AFE5C LD A,(SCFE)
AE4A FEAB CP A0
AE4C C2A73E JP NZ,3EA7
AE4F D31F OUT (1F),A
AE51 DBFF IN A,(FF)
AE53 E6C0 AND C0
AE55 28FA JR Z,AE51
AE57 17 RLA
AE58 3818 JR C,AE72
AE59 7E LD A,(HL)
AE5B 2F CPL
AE5C D37F OUT (7F),A
AE5E 23 INC HL
AE5F 18F0 JR AE51
AE61 15 DEC D
AE62 CA803E JP Z,3E80
AE65 D5 PUSH DE
AE68 CD913D CALL 3D91
AE69 3AF55C LD A,(SCF5)
AE6C CD0C3D CALL 3DCB
AE6F D1 POP DE
AE70 18CB JR AE3D
AE72 DB1F IN A,(1F)
AE74 D1 POP DE
AE75 47 LD B,A
AE76 E6FC AND FC
AE78 C8 RET Z
AE79 E610 AND 10
AE7B 20E4 JR NZ,AE51
AE7D 15 DEC D
AE7E 20BD JR NZ,AE3D
AE80 78 LD A,B
AE81 E64A96 AND 40
AE83 21002F LD HL,3F90
AE86 210030 JR NZ,AE8B
AE88 DB3F IN A,(3F)
AE89 B7 OR A
AE8E 2005 JR NZ,AE55
AE90 DB5F IN A,(5F)
AE92 FE0A CP 0A
AE94 C8 RET Z
AE95 DF RST 18
AE96 21003F LD HL,3FA0
AE99 DF RST 18
AE9A DB3F IN A,(3F)
AE9C CD8A3E CALL 3E8A
AE9F 3E07 LD A,07
AEA1 32875D LD (500F),A
AEA4 C35E01 JP 015E
AEA7 D31F OUT (1F),A
AEA9 DBFF IN A,(FF)
AEA8 E6C0 AND C0
AEA9 28FA JR Z,AEA9
AEA7 17 RLA
AEA8 DA723E JP C,3E72
AEA9 DB7F IN A,(7F)
AEA5 2F CPL
AEA6 77 LD (HL),A
AEA7 23 INC HL
AEA8 18EF JR AEA9
AEA9 4F LD C,A
AEA8 6688 LD B,00
AEA9 CD0C0A JP 0ACD
AEA8 210000 LD HL,0000
AEA9 110000 LD DE,0000
AEA8 6600 LD B,00
AEA9 E5 PUSH HL
AEA9 4E LD C,(HL)
AEA9 EB EX DE,HL
AEA9 09 ADD HL,BC
AEA9 EB EX DE,HL
AEA9 E1 POP HL
AEA9 28 INC HL
AEA9 7C LD A,H
AEA9 FE0C CP 0C
AEA9 20F2 JR NZ,AEA9
AEA9 3A4B3F LD A,(3F4B)
AEA9 BE CP E
AEA9 C2E03E JP NZ,3EE0
AEA9 3A4C3F LD A,(3F4C)
AEA9 BA CP D
AEA9 C8 RET Z
AEA9 219E3F LD HL,3F9E
AEA9 DF RST 18
AEA9 76 HALT
AEA9 C01404 CALL 0414
AEA9 7E LD A,(HL)
AEA9 B7 OR A
AEA9 CFF02 JP Z,02FF
AEA9 FE01 CP 01
AEA9 CC0F04 CALL Z,040F
AEA9 C0 RET NZ
AEA9 18F0 JR AEE5

```

WRITE PROTECT

DISC ERROR

TRACK

TRAPITE NO FICHeros 7 BORRADOS

PROTECCION INTIPRADO VET D.O.S.

ELIMINAR

DISC ERROR

TRAPITE SI HA LIGADO CAT EL NO BYTES LIBRES

LD DE, 0010 ADD HL, DE RET

```

REF5 3EAA LD A,AA
REF7 32175D LD (5D17),A
REFA AF XOR A
REFB 1802 LR REFF
REFD 3EFF LD A,FF
REF7 32CE5C LD (5CCE),A
RF02 110900 LD DE,0009
RF05 0E01 LD B,01
RF07 21005B LD HL,5B00
RF0A 03A20B JP 03A2
RF0D E5 PUSH HL
RF0E ED5BF45C LD DE,(5CF4)
RF12 C0083F CALL 3F05
RF15 3AD85C LD A,(5CDB)
RF18 D1 POP DE
RF19 B7 OR A
RF1A 2809 JR Z,REF5
RF1C 4F LD C,A
RF1D 21005B LD HL,5B00
RF20 ED5C LDIR
RF22 18D1 JR REFF
    
```

3F22  
DIRECCION  
REAL

- AF23 CF → CAT  
2A → \*  
D1 → MOVE  
E6 → NEW  
D2 → ERASE  
EF → LOAD  
F8 → SAVE  
FE → RETURN  
C0 → USR  
BE → PEEK  
F4 → POKE  
D5 → MERGE  
F7 → RUN

REPERTORIO DE  
COMANDOS DE DISCO

ΔF31 B3			
ΔF32	03 2E "E"	ΔF42	02 48 "H"
	04 3D "D"		07 4C "L"
	05 52 "R"		07 54 "T"
	04 AF → CODE		07 75 "U"
	04 82		0A 10
	06 56 "V"		02
	08 51 "Q"		
ΔF40	0A 5C "I"		

RESTO  
DE LA DECODIFICA-  
CION DE  
COMANDOS

MENSAJES

```

RF4E 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
RF50 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
RF52 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
RF54 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
RF56 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
RF58 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
RF5A 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
RF5C 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
RF5E 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
RF60 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
RF62 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
RF64 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
RF66 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
RF68 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
RF6A 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
RF6C 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
RF6E 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
RF70 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
RF72 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
RF74 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
RF76 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
RF78 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
RF7A 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
RF7C 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
RF7E 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
RF80 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
RF82 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
RF84 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
RF86 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
RF88 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
RF8A 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
RF8C 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
RF8E 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
RF90 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
RF92 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
RF94 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
RF96 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
RF98 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
RF9A 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
RF9C 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
RF9E 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
    
```

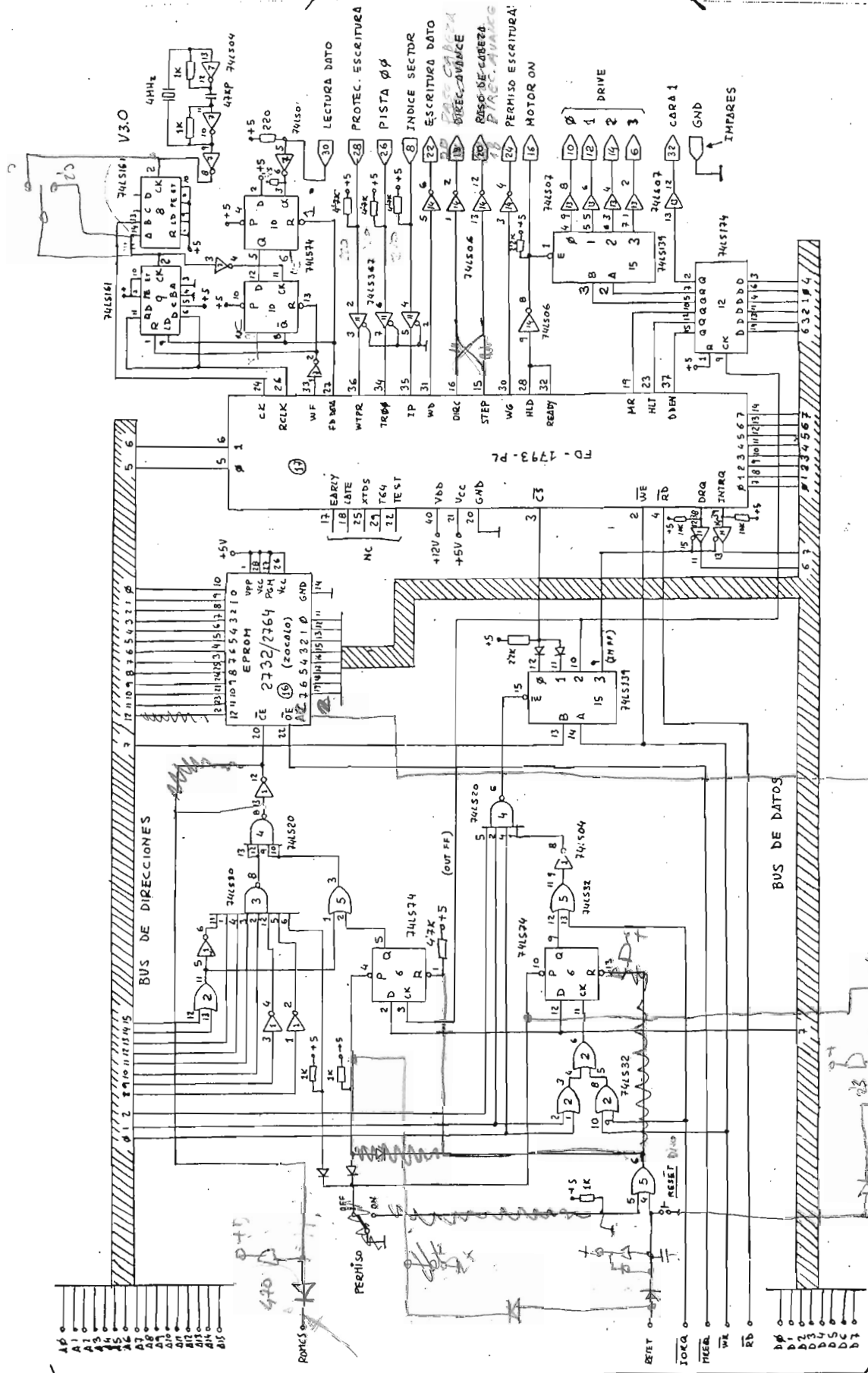
- 0b No file(s) 8D ←
- Del. File(s) 8D ←
- \* ERROR \* 8D ←
- No space. 8D ←
- File exists. 8D ←
- Free. 8D ←
- Write protect ←
- Disc Error ←
- Trk ←
- Rec. No. of ←
- Titulo: ←
- Nuevo clave: ←

- TITULO - 00  
FICHEROS =   
OD BORRADOS =

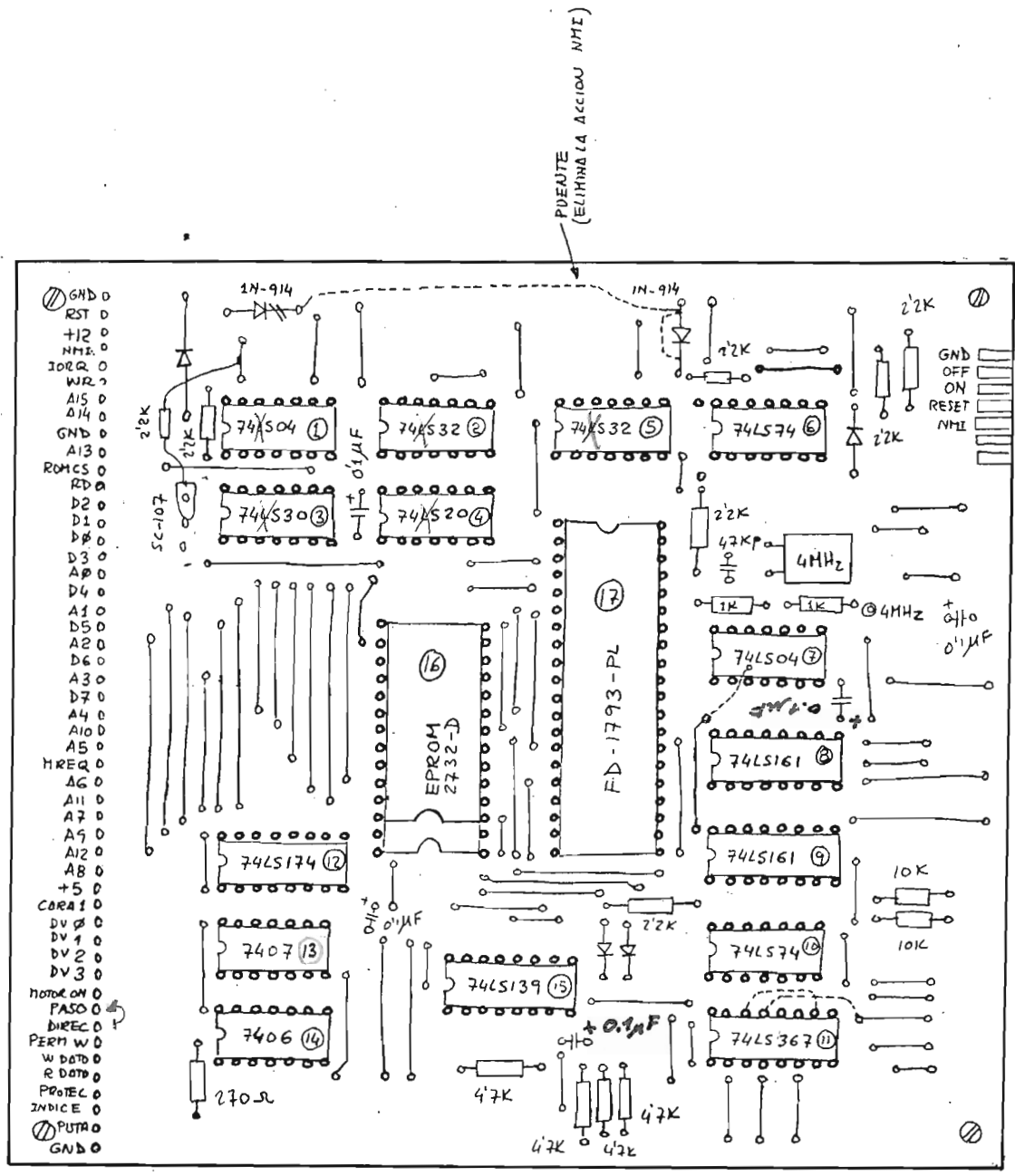
- 3FEF --- 1401 TITULO 1480
- 3F4D --- FICHEROS 8D
- 3F59 --- BORRADOS 8D
- 3F63 --- 0D 1201 ERROR 0D 1280
- 3F6E --- 0D NO CABE 8D
- 3F7B --- 0D YA EXISTE 8D
- 3F84 --- 0D NO EXISTE 8D
- 3F8F --- SECTORES LIBRES 8D
- 3F9A --- 0D DISCO PROTEGIDO
- 3FAB --- 0D ERROR DE DISCO
- 3FBB --- 0D - PISTA : A
- 3FCA --- NUEVA CLAVE :
- 3FD3 --- 0D DESBORRAMIENTO
- 3FE0 --- 1401 TITULO 1480

1

HACIA EL DRIVE



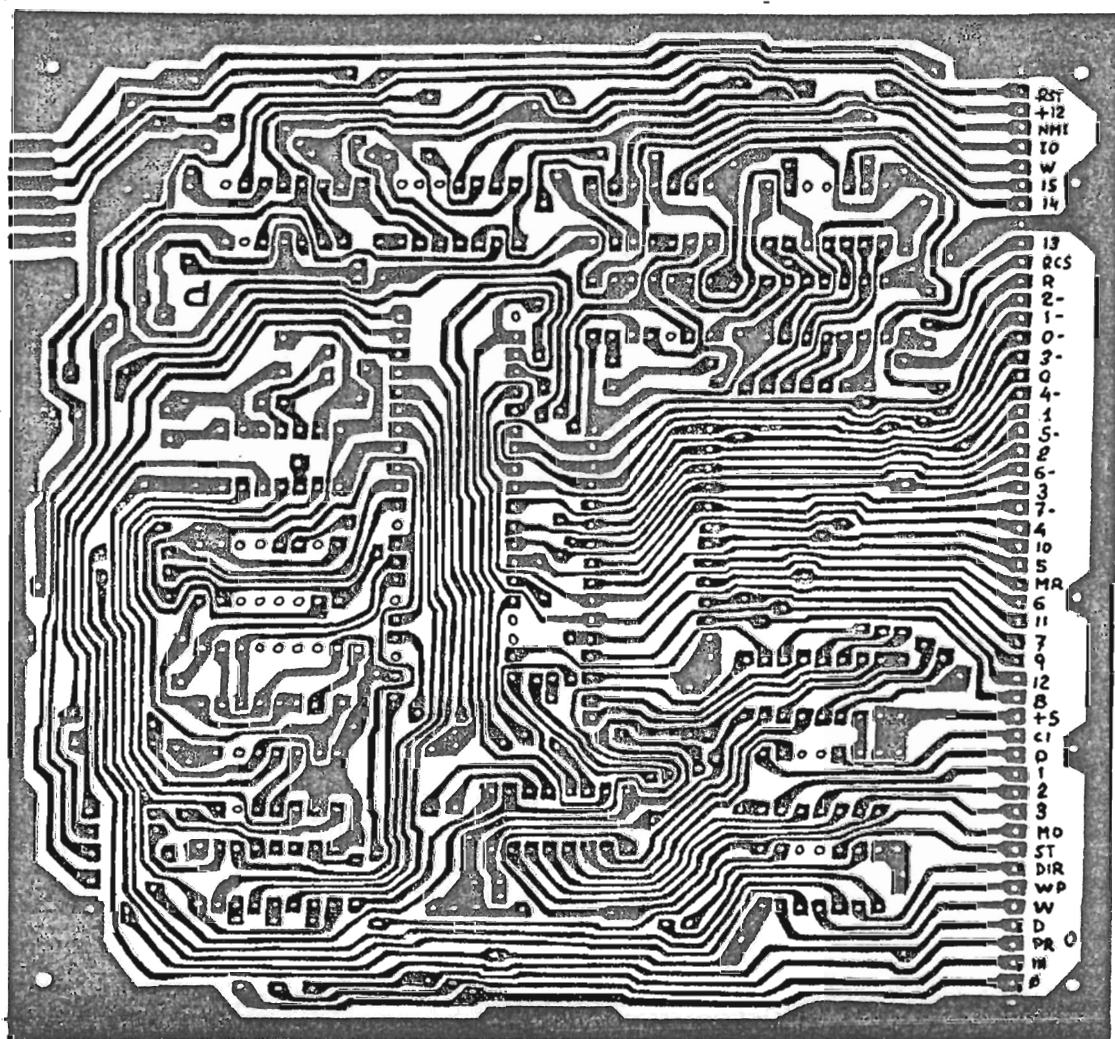
HACIA EL ORDENADOR



CARA DE COMPONENTES

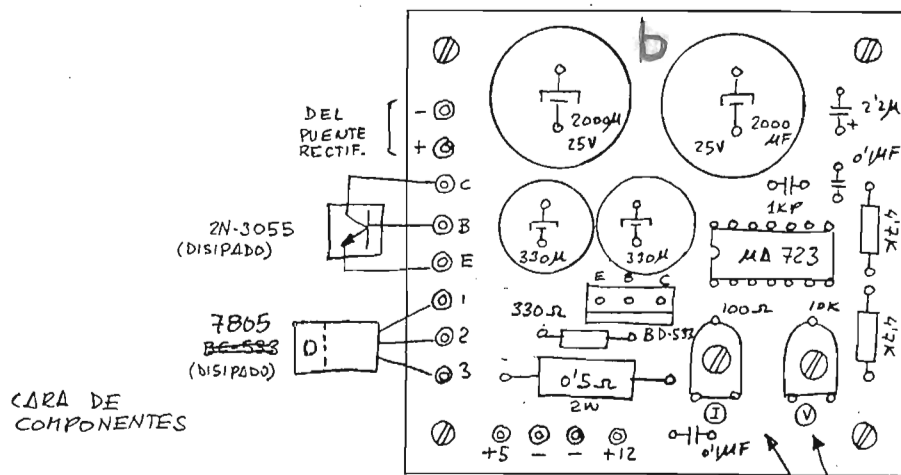
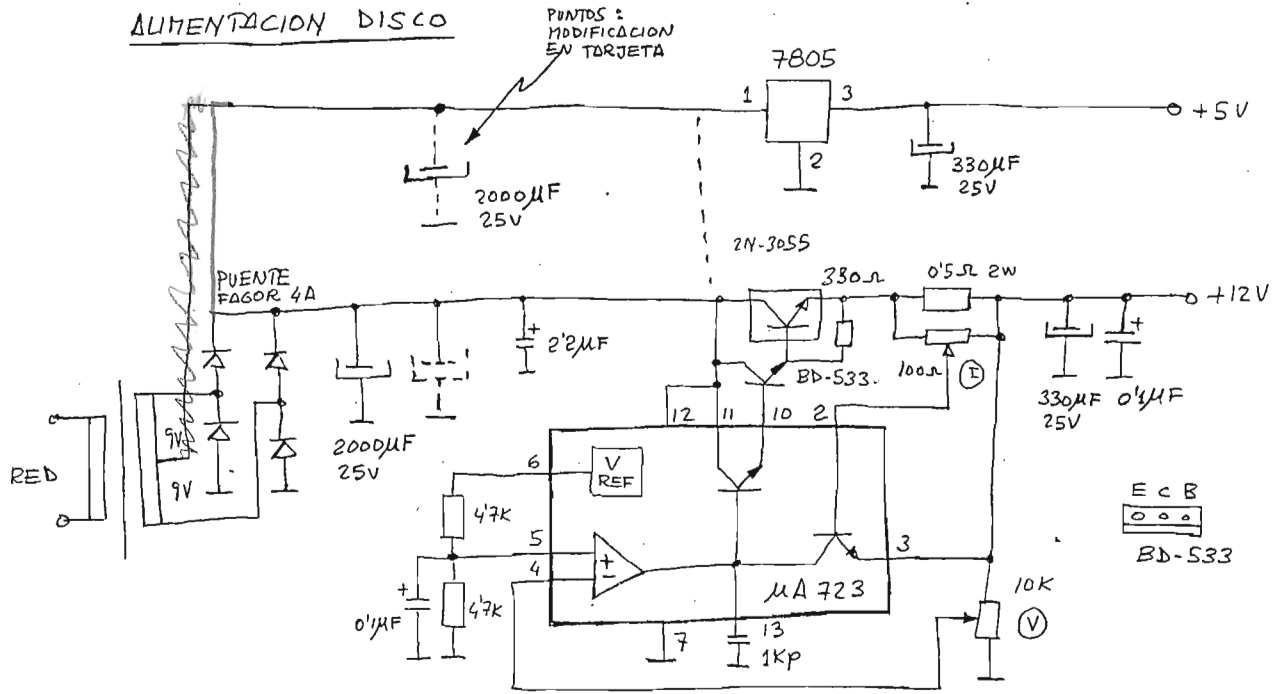




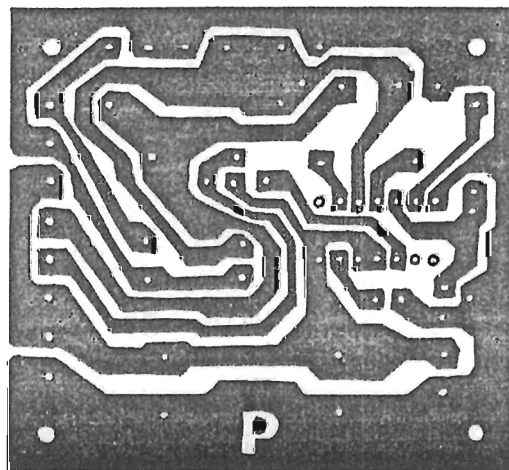


CARA DE PISTAS (TAMAÑO REAL)

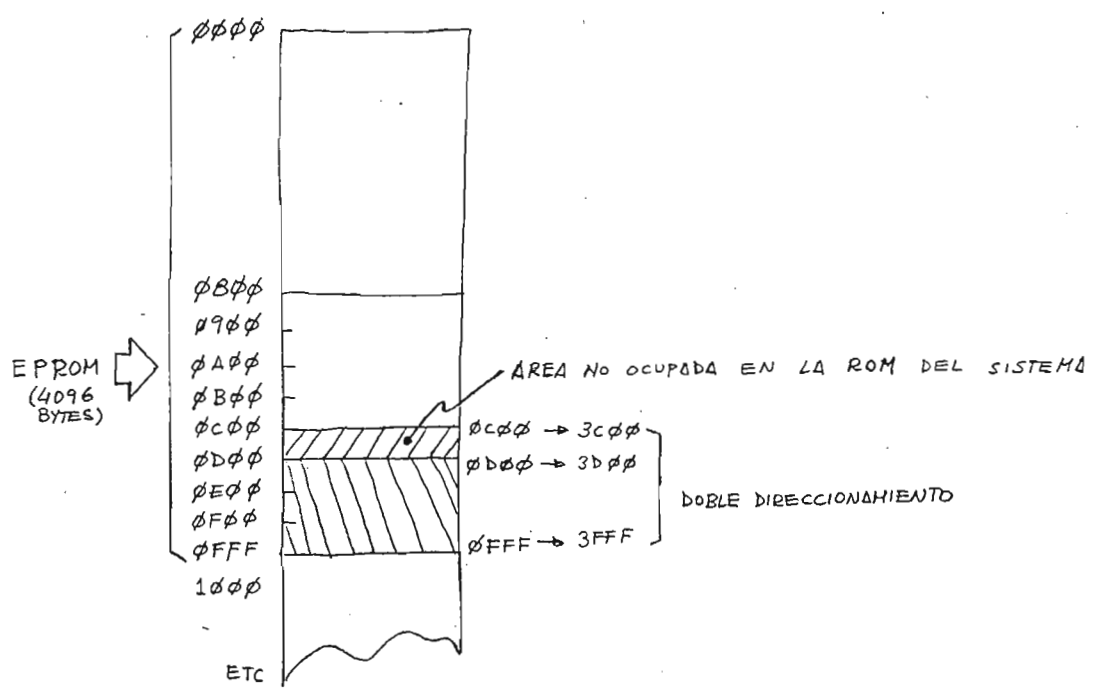
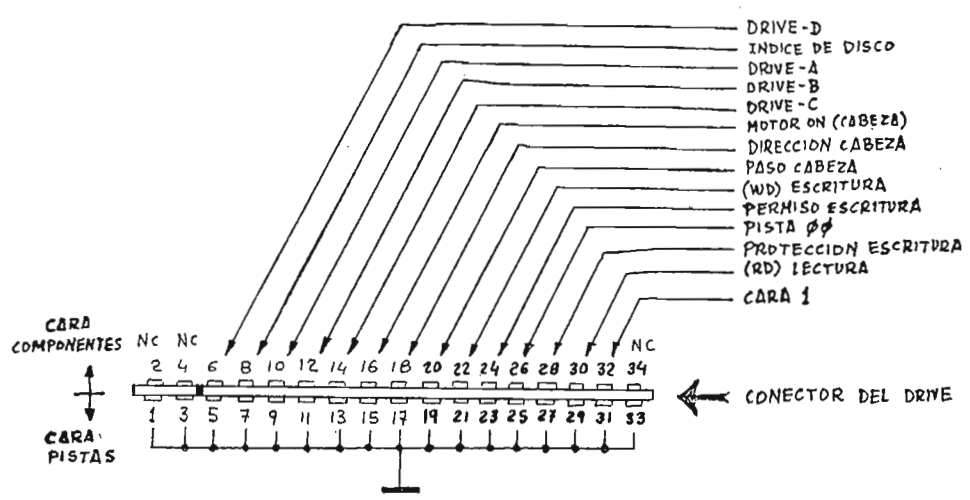
ALIMENTACION DISCO



POTENCIOMETROS DE AJUSTE V E I DE LA SALIDA 12V



CARA DE PISTAS



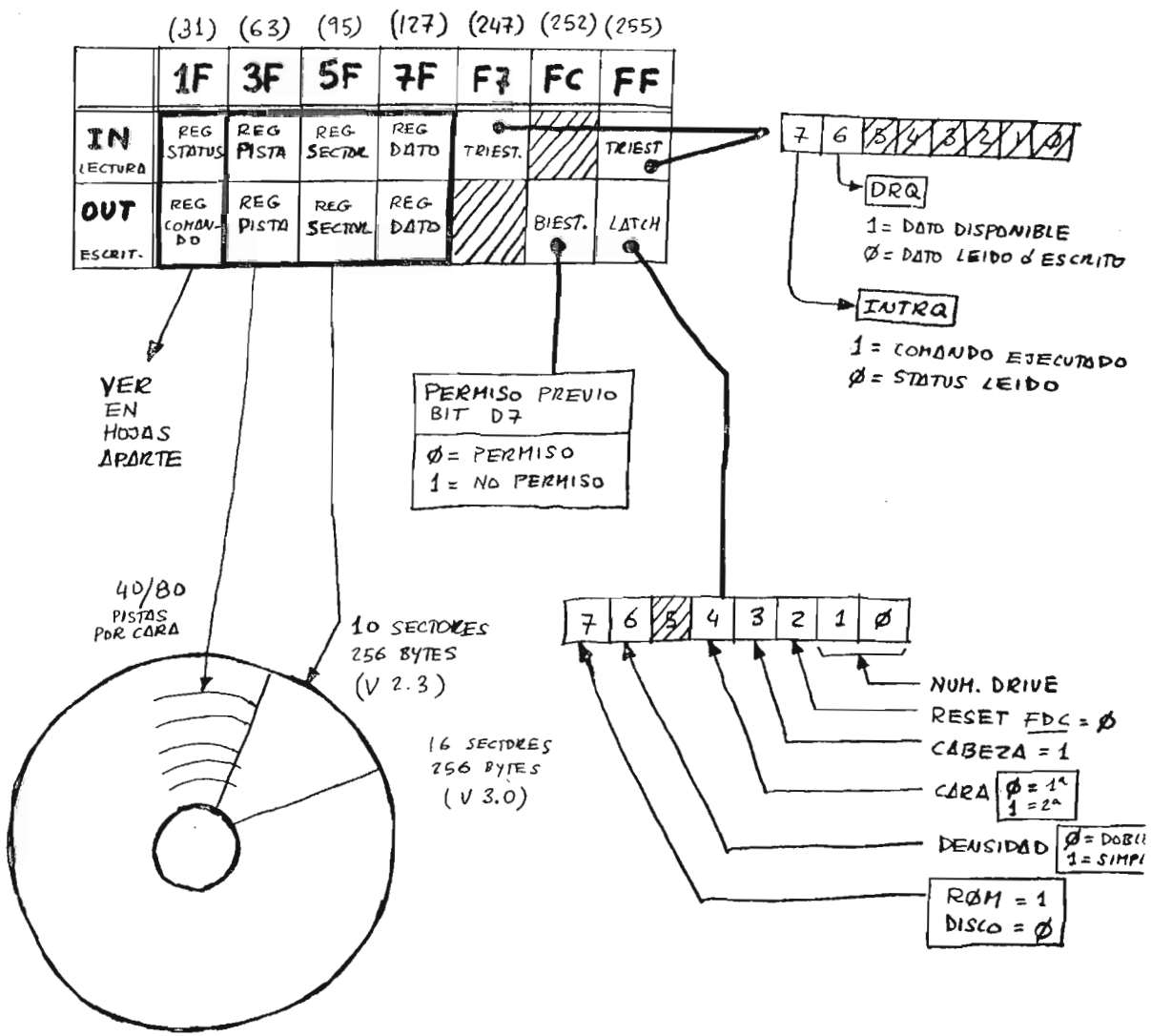
PAGINACION DEL D.O.S. LA PAGINACION OCUPA TODO LOS PRIMEROS 4 K BYTES DE LA ROM + 1 K BYTE DEL FINAL EN FORMA DE DOBLE DIRECCIONAMIENTO

D

1

A1 - A0	READ (RE)	WRITE (WE)
0 0	Status Register	Command Register
0 1	Track Register	Track Register
1 0	Sector Register	Sector Register
1 1	Data Register	Data Register

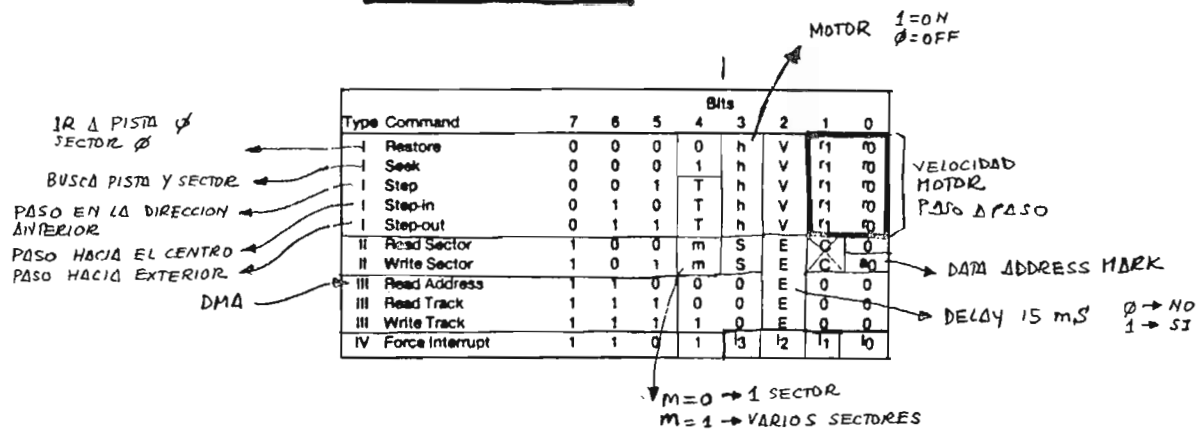
FILOSOFIA DE ACCESO A LOS REGISTROS



CAPACIDAD TOTAL = 409600 BYTES (V 2.3)  
 CAPACIDAD TOTAL = 655360 BYTES (V 3.0)

5D16 → GUARDA ESTADO LATCH

# COMANDOS



**FLAG SUMMARY**

Command Type	Bit No(s)	Description															
I	0, 1	1/0 = Stepping Motor Rate See Table 3 for Rate Summary															
I	2	V = Track Number Verify Flag V = 0, No verify V = 1, Verify on destination track															
I	3	h = Head Load Flag h = 1, Load head at beginning h = 0, Unload head at beginning															
I	4	T = Track Update Flag T = 0, No update T = 1, Update track register															
II	0	#0 = Data Address Mark #0 = 0, FB (DAM) #0 = 1, FB (deleted DAM)															
II	1	C = Side Compare Flag C = 0, Disable side compare C = 1, Enable side compare															
II & III	1	U = Update SSO U = 0, Update SSO to 0 U = 1, Update SSO to 1															
II & III	2	E = 15 MS Delay E = 0, No 15 MS delay E = 1, 15 MS delay															
II	3	S = Side Compare Flag S = 0, Compare for side 0 S = 1, Compare for side 1															
II	3	L = Sector Length Flag LSB's Sector Length in ID Field: <table border="1" style="font-size: small;"> <tr> <td></td> <td>00</td> <td>01</td> <td>10</td> <td>11</td> </tr> <tr> <td>L = 0</td> <td>256</td> <td>512</td> <td>1024</td> <td>128</td> </tr> <tr> <td>L = 1</td> <td>128</td> <td>256</td> <td>512</td> <td>1024</td> </tr> </table>		00	01	10	11	L = 0	256	512	1024	128	L = 1	128	256	512	1024
	00	01	10	11													
L = 0	256	512	1024	128													
L = 1	128	256	512	1024													
II	4	m = Multiple Record Flag m = 0, Single record m = 1, Multiple records															
IV	0-3	h <sub>i</sub> = Interrupt Condition Flags h <sub>0</sub> = 1 Not Ready To Ready Transition h <sub>1</sub> = 1 Ready To Not Ready Transition h <sub>2</sub> = 1 Index Pulse h <sub>3</sub> = 1 Immediate Interrupt, Requires A Reset h <sub>3</sub> h <sub>2</sub> h <sub>1</sub> h <sub>0</sub> = 0 Terminate With No Interrupt (INTRQ)															

CLK	2 MHz	2 MHz	1 MHz	1 MHz	2 MHz	1 MHz
DDEN	0	1	0	1	x	x
R1 R0	TEST=1	TEST=1	TEST=1	TEST=1	TEST=0	TEST=0
0 0	3 ms	3 ms	6 ms	6 ms	164µs	368µs
0 1	6 ms	6 ms	12 ms	12 ms	190µs	380µs
1 0	10 ms	10 ms	20 ms	20 ms	196µs	396µs
1 1	15 ms	15 ms	30 ms	30 ms	208µs	416µs

- RESTDRE → 00 MOTOR ON  
          00 MOTOR OFF
- SEEK → 10 MON  
          10 MOFF
- STEP → 20
- 20
- STEP IN → 48
- 40
- STEP OUT → 68
- 60
- R. SECT → B0
- W. SECT → A0
- R. TRACK → E0
- W. TRACK → F0
- INTERRUPT → D0 = NO INTERRUPCION

## RESUMEN

COMANDOS

# STATUS

3

BIT	ALL TYPE I COMMANDS	READ ADDRESS	READ SECTOR	READ TRACK	WRITE SECTOR	WRITE TRACK
S7	NOT READY	NOT READY	NOT READY	NOT READY	NOT READY	NOT READY
S6	WRITE PROTECT	0	0	0	WRITE PROTECT	WRITE PROTECT
S5	HEAD LOADED	0	RECORD TYPE	0	WRITE FAULT	WRITE FAULT
S4	SEEK ERROR	RNF	RNF	0	RNF	0
S3	CRC ERROR	CRC ERROR	CRC ERROR	0	CRC ERROR	0
S2	TRACK 0	LOST DATA	LOST DATA	LOST DATA	LOST DATA	LOST DATA
S1	INDEX PULSE	DRQ	DRQ	DRQ	DRQ	DRQ
S0	BUSY	BUSY	BUSY	BUSY	BUSY	BUSY

### STATUS FOR TYPE I COMMANDS

BIT NAME	MEANING
S7 NOT READY	This bit when set indicates the drive is not ready. When reset it indicates that the drive is ready. This bit is an inverted copy of the Ready input and logically 'ored' with MR.
S6 PROTECTED	When set, indicates Write Protect is activated. This bit is an inverted copy of WRPT input.
S5 HEAD LOADED	When set, it indicates the head is loaded and engaged. This bit is a logical "and" of HLD and HLT signals.
S4 SEEK ERROR	When set, the desired track was not verified. This bit is reset to 0 when updated.
S3 CRC ERROR	CRC encountered in ID field.
S2 TRACK 00	When set, indicates Read/Write head is positioned to Track 0. This bit is an inverted copy of the TROO input.
S1 INDEX	When set, indicates index mark detected from drive. This bit is an inverted copy of the IP input.
S0 BUSY	When set command is in progress. When reset no command is in progress.

### STATUS FOR TYPE II AND III COMMANDS

BIT NAME	MEANING
S7 NOT READY	This bit when set indicates the drive is not ready. When reset, it indicates that the drive is ready. This bit is an inverted copy of the Ready input and 'ored' with MR. The Type II and III Commands will not execute unless the drive is ready.
S6 WRITE PROTECT	On Read Record: Not Used. On Read Track: Not Used. On any Write: It indicates a Write Protect. This bit is reset when updated.
S5 RECORD TYPE/ WRITE FAULT	On Read Record: It indicates the record-type code from data field address mark. 1 = Deleted Data Mark. 0 = Data Mark. On any Write: It indicates a Write Fault. This bit is reset when updated.
S4 RECORD NOT FOUND (RNF)	When set, it indicates that the desired track, sector, or side were not found. This bit is reset when updated.
S3 CRC ERROR	If S4 is set, an error is found in one or more ID fields; otherwise it indicates error in data field. This bit is reset when updated.
S2 LOST DATA	When set, it indicates the computer did not respond to DRQ in one byte time. This bit is reset to zero when updated.
S1 DATA REQUEST	This bit is a copy of the DRQ output. When set, it indicates the DR is full on a Read Operation or the DR is empty on a Write operation. This bit is reset to zero when updated.
S0 BUSY	When set, command is under execution. When reset, no command is under execution.



```

A0003 F0008010E SET 1, (IY+01)
A0007 21070E LD HL, 0E0F
A000A 0008E2A CALL 2AB8E
A000C 2188E5C LD HL, 505B
A000E 328E2 LD (HL), 02
A0010 218E12 LD HL, 128B
A0013 218E12 LD HL, 128B
A0016 003793C LJP 3079
A0019 000413D CALL 3041
A001C 0008021 CALL 2180
A001F 0008E2A CALL 2AB8E
A0022 218E5C LD HL, (5059)
A0025 218E5C LD A, (HL)
A0028 218E5C CP AA
A002B 218E5C JR NZ, A0F1
A002E 218E5C INC HL
A0031 218E5C LD E, (HL)
A0034 218E5C INC HL
A0037 218E5C LD D, (HL)
A003A 218E5C EX DE, HL
A003D 218E5C JR A0F4
A0040 218E5C LD HL, 0081
A0043 218E5C LD (5042), HL
A0046 218E5C XOR A
A0049 218E5C LD (5044), A
A004C 218E5C LD HL, 15B0
A004F 0008E2A CALL 2AB8E
A0052 218E5C LD HL, (5053)
A0055 218E5C DEC HL
A0058 218E5C LD (5057), HL
A005B 218E5C LD HL, 301B
A005E 0008E2A CALL 2AB8E
A0061 000413D CALL 3041
A0064 218E5C LD A, FF
A0067 218E5C LD (5015), A
A006A 218E5C XOR A
A006D 218E5C LD (50F7), A
A0070 0008E2A CALL 3006
A0073 218E5C LD A, AA
A0076 218E5C LD (5017), A
A0079 218E5C LD HL, 217E
A007C 218E5C LD (501A), HL
A007F 218E5C LD HL, 0000
A0082 218E5C ADD HL, SP
A0085 218E5C LD (501C), HL
A0088 218E5C DEC HL
A008B 218E5C DEC HL
A008E 218E5C LD SP, HL
A0091 0008E2A CALL 21A8
A0094 218E5C LD HL, (505D)
A0097 0008E2A CALL 2155
A009A 218E5C JP NZ, 215E
A009D 218E5C CP AA
A00A0 218E5C INC HL
A00A3 218E5C JR NZ, A138
A00A6 0008E2A CALL 2155
A00A9 218E5C JR NZ, A138
A00AC 218E5C CP 3A
A00AF 218E5C JP NZ, 215E
A00B2 218E5C INC HL
A00B5 218E5C LD A, (HL)
A00B8 218E5C LD (5011), HL
A00BB 218E5C JR 21E
A00BE 218E5C LD A, (HL)
A00C1 218E5C CP 00
A00C4 218E5C RET NZ
A00C7 218E5C CP 00
A00CA 218E5C RET NZ
A00CD 218E5C CP A
A00D0 218E5C RET
A00D3 000413D CALL 3041
A00D6 218E5C LD A, (5017)
A00D9 218E5C JR A
A00DC 218E5C JR NZ, A16A
A00DF 000413F CALL 30714
A00E2 0008E2A CALL 2B550
A00E5 0008E2A CALL 2190
A00E8 218E5C LD SP, (501C)
A00EB 218E5C LD HL, (501A)
A00EE 218E5C LD BC, (500F)
A00F1 218E5C LD B, 00
A00F4 218E5C CP HL

```



```

A117E C0B0021 CALL 21B0
A1181 700B007E BIT 7, (1Y+00)
A1185 0000000 RET NZ
A1188 0000000 LD HL, (50B3)
A1189 0000000 LD (50B5), HL
A1190 0000000 PUSH HL
A1191 0000000 LD HL, 5092
A1192 0000000 LD (50B6), HL
A1193 0000000 POP HL
A1194 0000000 LD HL, 30BE
A1195 0000000 LD SP, (503D)
A1196 0000000 PUSH SP
A1197 0000000 RET
A1198 0000000 CALL 2AAE
A1199 0000000 CP 00
A11A0 0000000 RET NZ
A11A1 0000000 CALL 2A73
A11A2 0000000 JR 219D
A11A3 0000000 LD HL, (5030)
A11A4 0000000 LD (5013), HL
A11A5 0000000 LD HL, (501C)
A11A6 0000000 DEC HL
A11A7 0000000 DEC HL
A11A8 0000000 LD (503D), HL
A11A9 0000000 LD DE, 300F
A11AA 0000000 LD (HL), E
A11AB 0000000 INC HL
A11AC 0000000 LD (HL), D
A11AD 0000000 RET
A11AE 0000000 LD HL, (5013)
A11AF 0000000 LD (503D), HL
A11B0 0000000 RET
A11C4 0000000 LD HL, 0000
A11C7 0000000 LD (50F7), HL
A11C8 0000000 ADD HL, SP
A11C9 0000000 LD (501C), HL
A11CA 0000000 DEC HL
A11CB 0000000 DEC HL
A11CC 0000000 LD SP, HL
A11CD 0000000 CALL 21A8
A11CE 0000000 LD HL, 5017
A11CF 0000000 LD A, (HL)
A11D0 0000000 JP NZ, 21F1
A11D1 0000000 LD (HL), A
A11D2 0000000 CALL 2A88
A11D3 0000000 CALL 2AAA
A11D4 0000000 LD HL, 2277
A11D5 0000000 RST 18
A11D6 0000000 LD HL, 3FEF
A11D7 0000000 RST 18
A11D8 0000000 CALL 3009
A11D9 0000000 CALL 2A0F → CLAVE
A11E1 0000000 LD HL, (501C)
A11E4 0000000 DEC HL
A11E5 0000000 DEC HL
A11E6 0000000 LD HL, 303D
A11E7 0000000 CALL 3041
A11E8 0000000 CALL 2A84
A11E9 0000000 CALL 2A77 ELIMINAR. (CLAVE) TESTEA
A11EA 0000000 XOR A
A11EB 0000000 LD (5015), A
A11EC 0000000 LD HL, 21F1
A11ED 0000000 LD (501A), HL
A11EE 0000000 CALL 3006
A11EF 0000000 CALL 3080
A11F0 0000000 XOR A
A11F1 0000000 LD (500F), A
A11F2 0000000 LD HL, (5059)
A11F3 0000000 LD (5011), HL
A11F4 0000000 LD A, (HL)
A11F5 0000000 CP 00
A11F6 0000000 JR NZ, 220D
A11F7 0000000 LD HL, (501F)
A11F8 0000000 DEC HL
A11F9 0000000 LD 00, 00
A11FA 0000000 INC 00
A11FB 0000000 LD 00, A
A11FC 0000000 LD SP, (50B3)
A11FD 0000000 CP 00
A11FE 0000000 JP NZ, 215E
A11FF 0000000 LD 00, 0
A1200 0000000 INC HL
A1201 0000000 CP (HL)
A1202 0000000 JR NZ, 2225

```

```

0000 0000 0000 0000
0001 0000 0000 0000
0002 0000 0000 0000
0003 0000 0000 0000
0004 0000 0000 0000
0005 0000 0000 0000
0006 0000 0000 0000
0007 0000 0000 0000
0008 0000 0000 0000
0009 0000 0000 0000
0010 0000 0000 0000
0011 0000 0000 0000
0012 0000 0000 0000
0013 0000 0000 0000
0014 0000 0000 0000
0015 0000 0000 0000
0016 0000 0000 0000
0017 0000 0000 0000
0018 0000 0000 0000
0019 0000 0000 0000
0020 0000 0000 0000
0021 0000 0000 0000
0022 0000 0000 0000
0023 0000 0000 0000
0024 0000 0000 0000
0025 0000 0000 0000
0026 0000 0000 0000
0027 0000 0000 0000
0028 0000 0000 0000
0029 0000 0000 0000
0030 0000 0000 0000
0031 0000 0000 0000
0032 0000 0000 0000
0033 0000 0000 0000
0034 0000 0000 0000
0035 0000 0000 0000
0036 0000 0000 0000
0037 0000 0000 0000
0038 0000 0000 0000
0039 0000 0000 0000
0040 0000 0000 0000
0041 0000 0000 0000
0042 0000 0000 0000
0043 0000 0000 0000
0044 0000 0000 0000
0045 0000 0000 0000
0046 0000 0000 0000
0047 0000 0000 0000
0048 0000 0000 0000
0049 0000 0000 0000
0050 0000 0000 0000
0051 0000 0000 0000
0052 0000 0000 0000
0053 0000 0000 0000
0054 0000 0000 0000
0055 0000 0000 0000
0056 0000 0000 0000
0057 0000 0000 0000
0058 0000 0000 0000
0059 0000 0000 0000
0060 0000 0000 0000
0061 0000 0000 0000
0062 0000 0000 0000
0063 0000 0000 0000
0064 0000 0000 0000
0065 0000 0000 0000
0066 0000 0000 0000
0067 0000 0000 0000
0068 0000 0000 0000
0069 0000 0000 0000
0070 0000 0000 0000
0071 0000 0000 0000
0072 0000 0000 0000
0073 0000 0000 0000
0074 0000 0000 0000
0075 0000 0000 0000
0076 0000 0000 0000
0077 0000 0000 0000
0078 0000 0000 0000
0079 0000 0000 0000
0080 0000 0000 0000
0081 0000 0000 0000
0082 0000 0000 0000
0083 0000 0000 0000
0084 0000 0000 0000
0085 0000 0000 0000
0086 0000 0000 0000
0087 0000 0000 0000
0088 0000 0000 0000
0089 0000 0000 0000
0090 0000 0000 0000
0091 0000 0000 0000
0092 0000 0000 0000
0093 0000 0000 0000
0094 0000 0000 0000
0095 0000 0000 0000
0096 0000 0000 0000
0097 0000 0000 0000
0098 0000 0000 0000
0099 0000 0000 0000
0100 0000 0000 0000

```

```

XOR   A, A
LD    HL, (500F), A
LD    HL, (5005), A
LD    HL, (5010), A
LD    HL, 503B, A
RES   7, (HL)
LD    HL, 00
LD    HL, (5021)
DEC   C
SFLD C
ADD   HL, 0C
LD    HL, (HL)
INC   HL
LD    HL, (HL)
RXL   HL, HL
PUSH  HL, HL
LD    HL, R255
PUSH  HL
JP    HL
LD    HL, 503B
RST   7, (HL)
POP   HL
JP    HL
CALL  0095
CALL  0040
LD    HL, 3FE1 } "NUEVA CLAVE"
RST   13
CALL  00CF
LD    HL, 505A
LD    HL, 500B
LD    HL, 0009
LDIR
JP    303B

```

```

0101 0000 0000 0000
0102 0000 0000 0000
0103 0000 0000 0000
0104 0000 0000 0000
0105 0000 0000 0000
0106 0000 0000 0000
0107 0000 0000 0000
0108 0000 0000 0000
0109 0000 0000 0000
0110 0000 0000 0000
0111 0000 0000 0000
0112 0000 0000 0000
0113 0000 0000 0000
0114 0000 0000 0000
0115 0000 0000 0000
0116 0000 0000 0000
0117 0000 0000 0000
0118 0000 0000 0000
0119 0000 0000 0000
0120 0000 0000 0000
0121 0000 0000 0000
0122 0000 0000 0000
0123 0000 0000 0000
0124 0000 0000 0000
0125 0000 0000 0000
0126 0000 0000 0000
0127 0000 0000 0000
0128 0000 0000 0000
0129 0000 0000 0000
0130 0000 0000 0000
0131 0000 0000 0000
0132 0000 0000 0000
0133 0000 0000 0000
0134 0000 0000 0000
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0137 0000 0000 0000
0138 0000 0000 0000
0139 0000 0000 0000
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0180 0000 0000 0000
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0185 0000 0000 0000
0186 0000 0000 0000
0187 0000 0000 0000
0188 0000 0000 0000
0189 0000 0000 0000
0190 0000 0000 0000
0191 0000 0000 0000
0192 0000 0000 0000
0193 0000 0000 0000
0194 0000 0000 0000
0195 0000 0000 0000
0196 0000 0000 0000
0197 0000 0000 0000
0198 0000 0000 0000
0199 0000 0000 0000
0200 0000 0000 0000

```

```

LD    HL, (5059)
LD    HL, (HL), R2
INC   HL
LD    HL, (505B), HL
LD    HL, (HL), R2
INC   HL
LD    HL, 00
INC   HL
LD    HL, 00
INC   HL
LD    HL, 00
RST   7
CALL  0087
LD    HL, 0083
CALL  0044
LD    HL, 3FE5 } "CLAVE"
CALL  0089
LD    HL, 5059
INC   HL
LD    HL, 00
LD    HL, 00
LD    HL, 500B
LD    HL, (HL)
OR    HL, R2E0
LD    HL, (HL), A
PUSH  HL, C
LD    HL, R2F0
LD    HL, 00
LD    HL, 00
LD    HL, (DE), A
INC   HL
INC   HL
LD    HL, R2E7
RST   7
CALL  0048
CALL  30FF → "00"
CALL  30FF
LD    HL, (50E5)
CALL  2ACD
LD    HL, 3FAB → "FREE"
RST   13
JP    215E

```

```

R0316 0320F55D LD (500F),A
R0318 0321E55D LD A,(5015)
R031C 0322F3D ORR A
R0320 0323F3D CALL Z,3D2F
R0324 0324E3F RET
R0328 0325E3F LD HL,3F8C
R032C 0326E01 LD A,01
R0330 0327E29 JP 29A2
R0334 0328E XOR A
R0338 0329E LD (5000),A
R033C 032AE DE,(5000)
R0340 032BE LD D,00
R0344 032CE LD HL,5D17
R0348 032DE XOR A
R034C 032EE CP (HL)
R0350 032FE LD (HL),A
R0354 0330E JR Z,A340
R0358 0331E PUSH DE
R035C 0332E CALL 3F10
R0360 0333E POP DE
R0364 0334E LD HL,5B00
R0368 0335E LD B,01
R036C 0336E JP 3391
R0370 0337E LD DE,0008
R0374 0338E JR 3333
R0378 0339E CALL 3343
R037C 033AE LD A,(5BE7)
R0380 033BE CP 08
R0384 033CE JR C,A35B
R0388 033DE CP 11
R038C 033EE JR C,A351
R0390 033FE LD HL,3FBD
R0394 0340E RST 18
R0398 0341E JR 3313
R039C 0342E LD BC,(5CF5)
R03A0 0343E LD HL,5004
R03A4 0344E ADD HL,BC
R03A8 0345E LD (HL),A
R03AC 0346E LD A,(5BE3)
R03B0 0347E INC HL
R03B4 0348E INC HL
R03B8 0349E INC HL
R03BC 034AE LD (HL),A
R03C0 034BE LD HL,5006
R03C4 034CE LD DE,5BBA
R03C8 034DE LD (HL),DE
R03CC 034EE CALL 333E
R03D0 034FE RET
R03D4 0350E CALL 330F
R03D8 0351E JR 3340
R03DC 0352E LD HL,(5D11)
R03E0 0353E INC HL
R03E4 0354E LD A,(HL)
R03E8 0355E CP 00
R03EC 0356E JP NZ,239A
R03F0 0357E CALL 3304
R03F4 0358E CALL 3306
R03F8 0359E CALL 3308
R03FC 035AE XOR DE,HL
R0400 035BE CALL 330E
R0404 035CE CALL 330E
R0408 035DE CALL 3340
R040C 035EE CALL 3308
R0410 035FE CALL 3308
R0414 0360E LD HL,3FDA
R0418 0361E RST 18
R041C 0362E LD HL,5BFB
R0420 0363E RST 18
R0424 0364E CALL 3CFF
R0428 0365E LD A,(5BE4)
R042C 0366E LD HL,5BF4
R0430 0367E SUB (HL)
R0434 0368E PUSH HL
R0438 0369E CALL 3ED3
R043C 036AE LD HL,3F8F
R0440 036BE RST 18
R0444 036CE POP HL
R0448 036DE LD C,(HL)
R044C 036EE CALL 3ED4
R0450 036FE LD HL,3F78
R0454 0370E RST 18
R0458 0371E CALL 3329
R045C 0372E LD HL,5B00
R0460 0373E CALL 3F04
R0464 0374E CALL 3CFF
R0468 0375E LD A,(5CF6)
R046C 0376E ADD A,41
R0470 0377E RST 18
R0474 0378E LD B,02
R0478 0379E CALL 3F04

```

"No FILE"  
3F8F

"DISK ERROR"

ca 44 44

"TITULO"

"NONBRE"

"FILES"

"DEL FILES"

3EFG (NO PONER PRIMER0)

"A"

→ IMPRIME "00"

SUSTITUIR  
PARA  
ORDENAR EL  
ORDEN DE  
TITULO =  
NONBRE =









A77100	F71	P00P	IF
A77101	0044	CALL	DN, 2707
A77102	0727	P00P	DN
A77103	001	P00P	DN
A77104	000	RET	
A77105	47	P00P	
A77106	00037	CALL	DN, 488
A77107	0724	CALL	DN, 731
A77108	0000	CALL	DN, 12
A77109	1200	CALL	DN, 77
A77110	0077	PUSH	DN, 2001
A77111	0000	CALL	DN, (2001)
A77112	0000	CALL	DN, (2001)
A77113	0000	CALL	DN, (2001)
A77114	0000	CALL	DN, (2001)
A77115	0000	CALL	DN, (2001)
A77116	0000	CALL	DN, (2001)
A77117	0000	CALL	DN, (2001)
A77118	0000	CALL	DN, (2001)
A77119	0000	CALL	DN, (2001)
A77120	0000	CALL	DN, (2001)
A77121	0000	CALL	DN, (2001)
A77122	0000	CALL	DN, (2001)
A77123	0000	CALL	DN, (2001)
A77124	0000	CALL	DN, (2001)
A77125	0000	CALL	DN, (2001)
A77126	0000	CALL	DN, (2001)
A77127	0000	CALL	DN, (2001)
A77128	0000	CALL	DN, (2001)
A77129	0000	CALL	DN, (2001)
A77130	0000	CALL	DN, (2001)
A77131	0000	CALL	DN, (2001)
A77132	0000	CALL	DN, (2001)
A77133	0000	CALL	DN, (2001)
A77134	0000	CALL	DN, (2001)
A77135	0000	CALL	DN, (2001)
A77136	0000	CALL	DN, (2001)
A77137	0000	CALL	DN, (2001)
A77138	0000	CALL	DN, (2001)
A77139	0000	CALL	DN, (2001)
A77140	0000	CALL	DN, (2001)
A77141	0000	CALL	DN, (2001)
A77142	0000	CALL	DN, (2001)
A77143	0000	CALL	DN, (2001)
A77144	0000	CALL	DN, (2001)
A77145	0000	CALL	DN, (2001)
A77146	0000	CALL	DN, (2001)
A77147	0000	CALL	DN, (2001)
A77148	0000	CALL	DN, (2001)
A77149	0000	CALL	DN, (2001)
A77150	0000	CALL	DN, (2001)







```

A979 006F0B CALL 0B6F
A97C 0DC30A CALL 0AC3
A97F 0B79 SET 7,C
A981 79 LD A,C
A982 002D25C LD (5CD2),A
A983 0002 JR NC,A989
A984 007 SCF
A985 006 RET
A986 000FC JR NZ,A987
A987 0000 INC HL
A988 0000 LD E,(HL)
A989 0000 INC HL
A990 0000 LD D,(HL)
A991 0000 INC HL
A992 0000 LD (5CD7),HL
A993 0000 LD (5CD8),DE
A994 0000 ADD HL,DE
A995 0000 LD (5CD9),HL
A996 0000 CALL 0B6F
A997 0000 CP 29
A998 0000 JR NZ,A989
A999 0000 RET
AA00 0000 LD HL,3F70 "NO SPACE"
AA01 0000 LD A,03
AA02 0000 CALL 0316
AA03 0000 JP 015E
AA04 0000 LD HL,3F7B "FILE EXISTS"
AA05 0000 LD A,02
AA06 0000 JR A9A3
AA07 0000 LD HL,5CDD
AA08 0000 LD B,08
AA09 0000 LD (HL),20
AA0A 0000 INC HL
AA0B 0000 DJNZ A9BA
AA0C 0000 CALL 0AD2
AA0D 0000 LD A,B
AA0E 0000 OR C
AA0F 0000 JP NZ,0A60
AA10 0000 EX DE,HL
AA11 0000 CALL 09DE
AA12 0000 LD A,C
AA13 0000 CP 09
AA14 0000 JR C,A9D2
AA15 0000 LD C,08
AA16 0000 LD A,(HL)
AA17 0000 CP 20
AA18 0000 JP C,0A60
AA19 0000 LD DE,5CDD
AA1A 0000 LD IR
AA1B 0000 RET
AA1C 0000 INC HL
AA1D 0000 LD A,(HL)
AA1E 0000 CP 3A
AA1F 0000 JR NZ,A9FE
AA20 0000 DEC HL
AA21 0000 LD A,(HL)
AA22 0000 AND 0F "1101 1111"
AA23 0000 SBC A,41
AA24 0000 JP C,0A60
AA25 0000 CP 04
AA26 0000 JP NC,0A60
AA27 0000 PUSH BC
AA28 0000 PUSH HL
AA29 0000 CALL 3DA3
AA2A 0000 POP HL
AA2B 0000 POP BC
AA2C 0000 DEC BC
AA2D 0000 DEC BC
AA2E 0000 INC HL
AA2F 0000 INC HL
AA30 0000 RET
AA31 0000 DEC HL
AA32 0000 LD A,(5D19)
AA33 0000 PUSH BC
AA34 0000 PUSH HL
AA35 0000 CALL 3DA9
AA36 0000 POP HL
AA37 0000 POP BC
AA38 0000 RET
AA39 0000 LD L,C
AA40 0000 LD H,00
AA41 0000 ADD HL,HL
AA42 0000 ADD HL,HL
AA43 0000 ADD HL,HL
AA44 0000 ADD HL,HL
AA45 0000 LD BC,5B00
AA46 0000 ADD HL,BC
AA47 0000 RET

```

IMPRESSION  
REAL

"NO SPACE"

"FILE EXISTS"

1101 1111

→



AD000	0150000	LD	HL, 0000
AD001	1070000	JR	AB0E
AD002	2100000	LD	HL, 000E
AD003	1070000	JR	AB0E
AD004	0015000	CALL	0015
AD005	0110000	LD	HL, 1A1B
AD006	0000000	JP	3ED9
AD007	0170000	LD	HL, 0BF1
AD008	1070000	JR	AB0E
AD009	2100000	LD	HL, 1E99
AD010	1000000	JR	AB0E
AD011	2100000	LD	HL, 1080
AD012	1000000	JR	AB0E
AD013	2100000	LD	HL, 1082
AD014	1000000	JR	AB0E
AD015	0011500	LD	HL, (5D11)
AD016	0000000	INC	HL
AD017	0000000	LD	(5C5D), HL
AD018	0000000	RET	
AD019	0000000	CALL	0000
AD020	0000000	CALL	0000
AD021	0000000	CALL	0000
AD022	0000000	CALL	0000
AD023	0000000	CALL	0000
AD024	0000000	CALL	0000
AD025	0000000	CALL	0000
AD026	0000000	CALL	0000
AD027	0000000	CALL	0000
AD028	0000000	CALL	0000
AD029	0000000	CALL	0000
AD030	0000000	CALL	0000
AD031	0000000	CALL	0000
AD032	0000000	CALL	0000
AD033	0000000	CALL	0000
AD034	0000000	CALL	0000
AD035	0000000	CALL	0000
AD036	0000000	CALL	0000
AD037	0000000	CALL	0000
AD038	0000000	CALL	0000
AD039	0000000	CALL	0000
AD040	0000000	CALL	0000
AD041	0000000	CALL	0000
AD042	0000000	CALL	0000
AD043	0000000	CALL	0000
AD044	0000000	CALL	0000
AD045	0000000	CALL	0000
AD046	0000000	CALL	0000
AD047	0000000	CALL	0000
AD048	0000000	CALL	0000
AD049	0000000	CALL	0000
AD050	0000000	CALL	0000
AD051	0000000	CALL	0000
AD052	0000000	CALL	0000
AD053	0000000	CALL	0000
AD054	0000000	CALL	0000
AD055	0000000	CALL	0000
AD056	0000000	CALL	0000
AD057	0000000	CALL	0000
AD058	0000000	CALL	0000
AD059	0000000	CALL	0000
AD060	0000000	CALL	0000
AD061	0000000	CALL	0000
AD062	0000000	CALL	0000
AD063	0000000	CALL	0000
AD064	0000000	CALL	0000
AD065	0000000	CALL	0000
AD066	0000000	CALL	0000
AD067	0000000	CALL	0000
AD068	0000000	CALL	0000
AD069	0000000	CALL	0000
AD070	0000000	CALL	0000
AD071	0000000	CALL	0000
AD072	0000000	CALL	0000
AD073	0000000	CALL	0000
AD074	0000000	CALL	0000
AD075	0000000	CALL	0000
AD076	0000000	CALL	0000
AD077	0000000	CALL	0000
AD078	0000000	CALL	0000
AD079	0000000	CALL	0000
AD080	0000000	CALL	0000
AD081	0000000	CALL	0000
AD082	0000000	CALL	0000
AD083	0000000	CALL	0000
AD084	0000000	CALL	0000
AD085	0000000	CALL	0000
AD086	0000000	CALL	0000
AD087	0000000	CALL	0000
AD088	0000000	CALL	0000
AD089	0000000	CALL	0000
AD090	0000000	CALL	0000
AD091	0000000	CALL	0000
AD092	0000000	CALL	0000
AD093	0000000	CALL	0000
AD094	0000000	CALL	0000
AD095	0000000	CALL	0000
AD096	0000000	CALL	0000
AD097	0000000	CALL	0000
AD098	0000000	CALL	0000
AD099	0000000	CALL	0000
AD100	0000000	CALL	0000

AB0000	22200250	LD	(5000), HL
AB0001	2150010	LD	HL, 1555
AB0002	1900000	JR	DB, 79
AB0003	1800000	XOR	A
AB0004	1800000	JR	AB03
AB0005	0D19225	CALL	2519
AB0006	ED0507450	LD	DE, (5CF4)
AB0007	10	DEC	B, 01
AB0008	05001	LD	HL, 01
AB0009	0210000	LD	HL, 5000
AB0010	0300000	LD	A, FF5000
AB0011	0300000	LD	(5000), A
AB0012	0300000	LD	(50CF4), DE
AB0013	0300000	XOR	D
AB0014	0300000	XOR	B
AB0015	0300000	PUSH	BC
AB0016	0300000	PUSH	DE
AB0017	0300000	PUSH	HL
AB0018	0300000	CALL	DE4E
AB0019	0300000	LD	DE, (5CF4)
AB0020	0300000	CALL	DE4A
AB0021	0300000	LD	DE, (5CF5)
AB0022	0300000	CALL	DEEB
AB0023	0300000	LD	DE, (50CE)
AB0024	0300000	LD	DE, 0000
AB0025	0300000	LD	DE, 3E56
AB0026	0300000	LD	DE, 3E52
AB0027	0300000	LD	DE, 0100
AB0028	0300000	LD	DE, DE
AB0029	0300000	PUSH	HL
AB0030	0300000	LD	DE, 5004
AB0031	0300000	LD	DE, (5CF5)
AB0032	0300000	LD	DE, DE
AB0033	0300000	LD	DE, (HL)
AB0034	0300000	LD	DE, 5CF4
AB0035	0300000	INC	(HL)
AB0036	0300000	LD	(HL)
AB0037	0300000	JR	NZ, AB05
AB0038	0300000	LD	(HL), 00
AB0039	0300000	LD	HL, 5CF5
AB0040	0300000	INC	(HL)
AB0041	0300000	LD	HL
AB0042	0300000	LD	BC
AB0043	0300000	JNZ	AB0D
AB0044	0300000	RET	
AB0045	0300000	PUSH	HL
AB0046	0300000	LD	HL, A
AB0047	0300000	LD	HL, 00
AB0048	0300000	PUSH	HL
AB0049	0300000	PUSH	HL, DE
AB0050	0300000	CALL	0, 2BFA
AB0051	0300000	LD	HL, H
AB0052	0300000	LD	HL
AB0053	0300000	LD	A, D
AB0054	0300000	LD	A, D
AB0055	0300000	XOR	A
AB0056	0300000	LD	(50D6), A
AB0057	0300000	LD	
AB0058	0300000	LD	



```

00000000 CALL 3CE0
00000001 OR 00
00000002 OUT (FC),A
00000003 RET
00000004 LD A,(5C48)
00000005 AND 33
00000006 RRCA
00000007 RRCA
00000008 RET
00000009 CALL 3C02
0000000A LD A,FF
0000000B OUT (FF),A
0000000C RET
0000000D CALL 3CE9
0000000E LD R
0000000F JR ACAD
00000010 CALL 3CE9
00000011 LD R
00000012 JR ACAD
00000013 LD A,80
00000014 PUSH HL
00000015 PUSH BC
00000016 CALL 3C015
00000017 CALL 3C007
00000018 CALL 3C023
00000019 POP BC
0000001A POP HL
0000001B RET
0000001C LD HL,0010
0000001D JP 3ABE
0000001E PUSH BC
0000001F LD HL,5B50
00000020 LD BC,0020
00000021 LD DE,5001
00000022 LDIR
00000023 POP BC
00000024 RET
00000025 LD HL,5C01
00000026 LD DE,5B50
00000027 LD BC,0020
00000028 LDIR
00000029 RET
0000002A LD A,(HL)
0000002B OR AN
0000002C RET NZ
0000002D AND 7F
0000002E RST 10
0000002F BIT 7,(HL)
00000030 RET NZ
00000031 INC HL
00000032 JR 3ABE
00000033 CALL 3B97
00000034 JP 15E
00000035 LD A,(5C65)
00000036 CP 74
00000037 RET N
00000038 LD HL,5018
00000039 OR (HL)
0000003A LD (HL),FF
0000003B RET NZ
0000003C LD HL,5066
0000003D LD DE,5026
0000003E LD BC,3A
0000003F LD (HL)
00000040 LD A,(DE)
00000041 LD (HL),A
00000042 LD A,C
00000043 LD (DE),A
00000044 INC HL
00000045 INC DE
00000046 DJNZ 3A58
00000047 RET
00000048 LD HL,(5C59)
00000049 LD (HL),80
0000004A LD (5C58),HL
0000004B INC HL
0000004C LD (HL),80
0000004D RET
0000004E LD A,(5D0F)
0000004F OR A
00000050 CALL NZ,3050
00000051 LD HL,(5C59)
00000052 CALL 3CFF
00000053 LD A,(5D19)
00000054 RST 44
00000055 RST 10
00000056 LD A,3E
00000057 RST 10
00000058 LD HL,5C3A
00000059 LD (HL),FF
0000005A CALL 3AB0
0000005B CALL 3AC0
0000005C RET

```





AD088E	1D	LD	A, (DE)
AD0897	00AD	CP	(HL)
AD0900	0000	RET	NZ
AD0901	1033	INC	DE
AD0902	0033	INC	HL
AD0903	10F9	CUNZ	AO8E
AD0905	0000	RET	
AD0907	0000	PUSH	BC
AD0909	0000	LD	B, 08
AD090A	0070	LD	A, (HL)
AD090B	0003	RST	10
AD090C	1003	INC	HL
AD090E	1003	CUNZ	AO99
AD090F	0000	LD	A, 3C
AD0910	0070	RST	10
AD0911	0070	LD	A, (HL)
AD0912	0003	RST	10
AD0913	0070	LD	A, 3E
AD0914	0001	RST	10
AD0915	0000	POP	BC
AD0917	0000	RET	
AD0918	0000	CALL	2085
AD0919	0000	CALL	2034D
AD091A	0000	JP	20A19
AD091B	1117	LD	DE, SCFA
AD091C	0000	LD	HL, (SCFB)
AD091D	1110	ADD	HL, DE
AD091E	0000	XOR	A
AD091F	0070	LD	(HL), A
AD0920	001E	LD	A, (501E)
AD0921	0017	OUT	(1F), A
AD0922	0000	IN	A, (FF)
AD0923	0000	AND	80
AD0924	0000	JR	N, ADBF
AD0925	0000	RET	
AD0926	0019	LD	A, (5019)
AD0927	0000	LD	(50FB), A
AD0928	0018	LD	HL, 5018
AD0929	0000	LD	C, A
AD092A	003C	LD	D, 3C
AD092B	0000	OR	C
AD092C	0000	OUT	(FF), A
AD092D	0070	LD	(HL), A
AD092E	11FA	LD	DE, SCFA
AD092F	0000	LD	HL, (50FB)
AD0930	0000	ADD	HL, DE
AD0931	0000	LD	A, (HL)
AD0932	0000	OUT	(3F), A
AD0933	0000	LD	A, 8F
AD0934	0000	LD	C, 7F
AD0935	0000	DEC	C
AD0936	0000	JR	NZ, ADE4
AD0937	0000	DEC	A
AD0938	0000	JR	NZ, ADE2
AD0939	0000	RET	
AD093A	0047	LD	C, A
AD093B	0000	IN	A, (1F)
AD093C	0000	AND	80
AD093D	0000	LD	(500D), A
AD093E	0000	LD	DE, (50FB)
AD093F	0000	LD	HL, SCFA
AD0940	0000	ADD	HL, DE
AD0941	0016	LD	A, (5016)
AD0942	0000	OR	3C
AD0943	0016	LD	(5016), A
AD0944	0000	OUT	(FF), A
AD0945	0000	LD	(HL), C
AD0946	0000	PUSH	HL
AD0947	0000	LD	HL, 5008
AD0948	0000	ADD	HL, DE
AD0949	0000	LD	A, (HL)
AD094A	0000	POP	HL
AD094B	0000	CALL	17
AD094C	0000	CALL	N, 3E38
AD094D	0000	CP	18
AD094E	0000	CALL	N, 3E38
AD094F	0000	LD	A, C
AD0950	0000	OUT	(7F), A
AD0951	001E	LD	A, (501E)
AD0952	0010	OR	10
AD0953	0000	OUT	(1F), A
AD0954	0000	LD	A, (500D)
AD0955	0000	OR	A
AD0956	0000	JR	N, AE30
AD0957	0000	LD	A, 80
AD0958	0000	LD	A, 80
AD0959	0000	LD	A, 80
AD095A	0000	CALL	30
AD095B	1070	CUNZ	AE00
AD095C	0000	CALL	308F
AD095D	0010	LD	A, 10
AD095E	0000	LD	308A

5B

5D





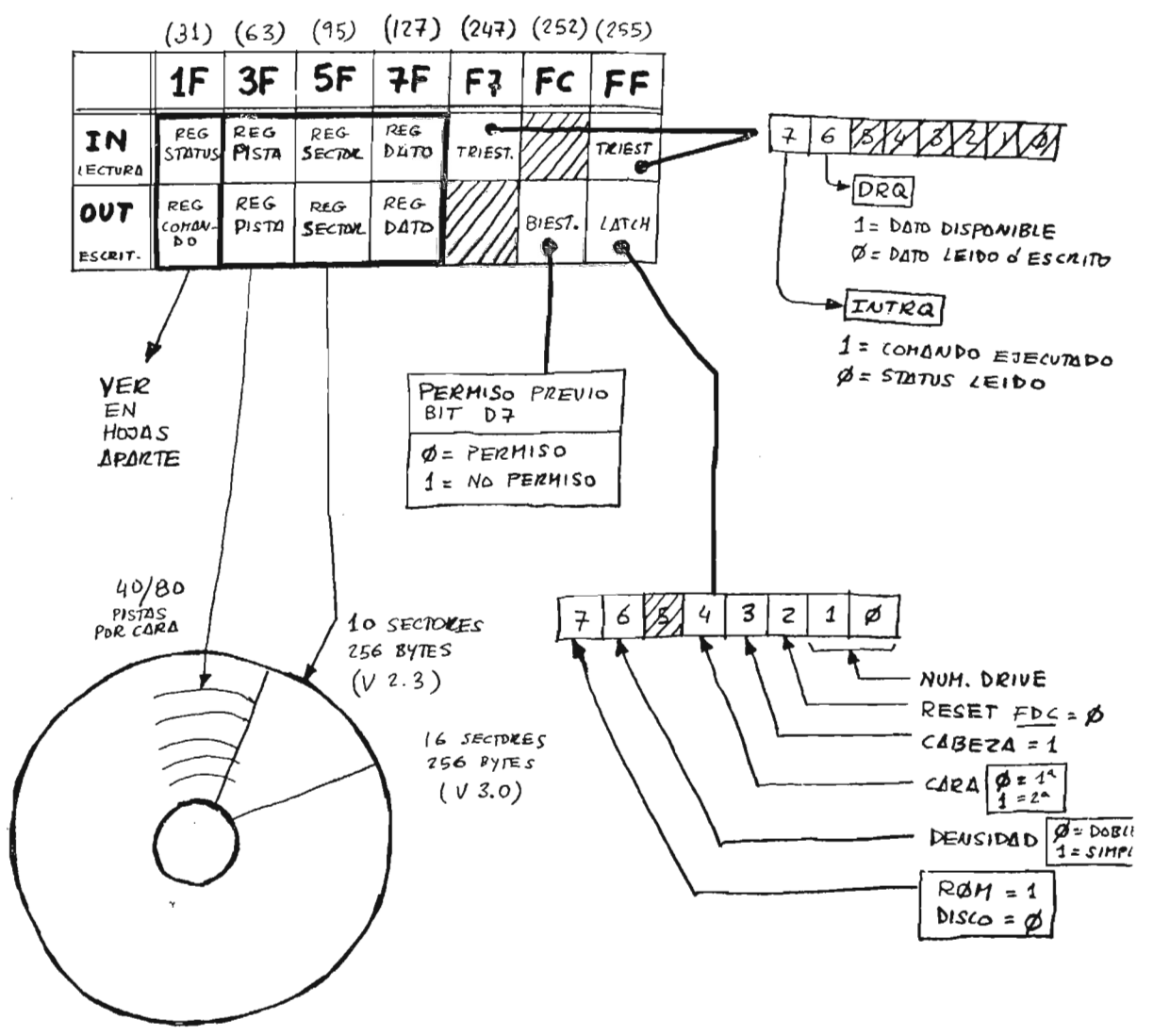


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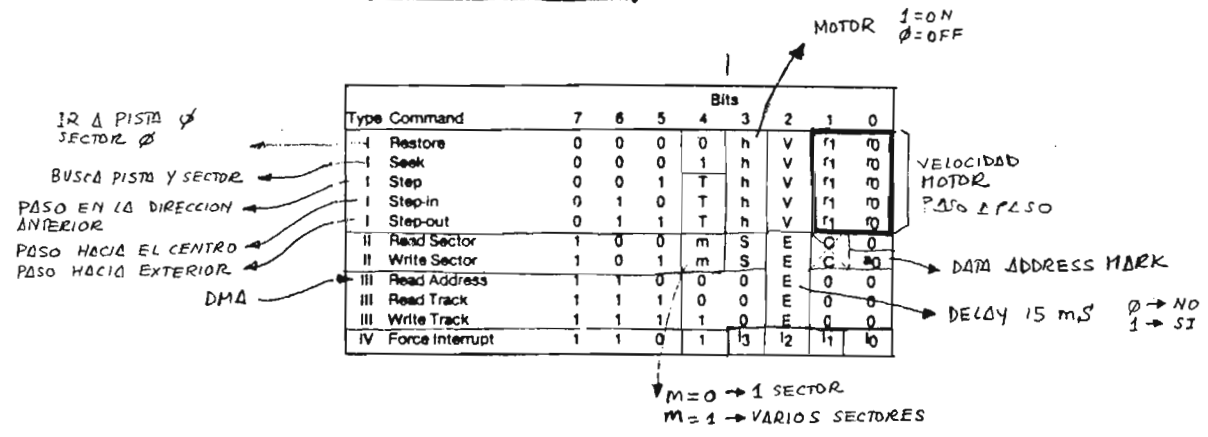
A1 - A0	READ (RE)	WRITE (WE)
0 0	Status Register	Command Register
0 1	Track Register	Track Register
1 0	Sector Register	Sector Register
1 1	Data Register	Data Register

FILOSOFIA DE ACCESO A LOS REGISTROS



CAPACIDAD TOTAL = 409600 BYTES (V 2.3)  
 CAPACIDAD TOTAL = 655360 BYTES (V 3.0)

# COMANDOS



## FLAG SUMMARY

Command Type	Bit No(s)	Description															
I	0, 1	f1'0 = Stepping Motor Rate See Table 3 for Rate Summary															
I	2	V = Track Number Verify Flag V = 0, No verify V = 1, Verify on destination track															
I	3	h = Head Load Flag h = 1, Load head at beginning h = 0, Unload head at beginning															
I	4	T = Track Update Flag T = 0, No update T = 1, Update track register															
II	0	#0 = Data Address Mark #0 = 0, FB (DAM) #0 = 1, FB (deleted DAM)															
II	1	C = Side Compare Flag C = 0, Disable side compare C = 1, Enable side compare															
II & III	1	U = Update SSO U = 0, Update SSO to 0 U = 1, Update SSO to 1															
II & III	2	E = 15 MS Delay E = 0, No 15 MS delay E = 1, 15 MS delay															
II	3	S = Side Compare Flag S = 0, Compare for side 0 S = 1, Compare for side 1															
II	3	L = Sector Length Flag LSB's Sector Length in ID Field: <table border="1" style="margin-left: 20px;"> <tr> <td></td> <td>00</td> <td>01</td> <td>10</td> <td>11</td> </tr> <tr> <td>L = 0</td> <td>256</td> <td>512</td> <td>1024</td> <td>120</td> </tr> <tr> <td>L = 1</td> <td>128</td> <td>256</td> <td>512</td> <td>1024</td> </tr> </table>		00	01	10	11	L = 0	256	512	1024	120	L = 1	128	256	512	1024
	00	01	10	11													
L = 0	256	512	1024	120													
L = 1	128	256	512	1024													
II	4	m = Multiple Record Flag m = 0, Single record m = 1, Multiple records															
IV	0-3	I <sub>x</sub> = Interrupt Condition Flags I <sub>0</sub> = 1 Not Ready To Ready Transition I <sub>1</sub> = 1 Ready To Not Ready Transition I <sub>2</sub> = 1 Index Pulse I <sub>3</sub> = 1 Immediate Interrupt, Requires A Reset I <sub>3-0</sub> = 0 Terminate With No Interrupt (INTRQ)															

CLK	2 MHz	2 MHz	1 MHz	1 MHz	2 MHz	1 MHz
DDEN	0	1	0	1	x	x
R1 R0	TEST=1	TEST=1	TEST=1	TEST=1	TEST=0	TEST=0
0 0	3 ms	3 ms	8 ms	8 ms	184µs	368µs
0 1	8 ms	8 ms	12 ms	12 ms	190µs	380µs
1 0	10 ms	10 ms	20 ms	20 ms	196µs	392µs
1 1	15 ms	15 ms	30 ms	30 ms	208µs	416µs

- RESTORE → 08 MOTDR ON  
00 MOTDR OFF
- SEEK → 18 MON  
10 MOFF
- STEP → 28  
20
- STEP IN → 48  
40
- STEP OUT → 68  
60
- R. SECT → B0
- W. SECT → A0
- R. TRACK → E0
- W. TRACK → F0
- INTERRUPT → D0 = NO INTERRUPTION

## RESUMEN COMANDOS

# STATUS

3

BIT	ALL TYPE I COMMANDS	READ ADDRESS	READ SECTOR	READ TRACK	WRITE SECTOR	WRITE TRACK
S7	NOT READY	NOT READY	NOT READY	NOT READY	NOT READY	NOT READY
S6	WRITE PROTECT	0	0	0	WRITE PROTECT	WRITE PROTECT
S5	HEAD LOADED	0	RECORD TYPE	0	WRITE FAULT	WRITE FAULT
S4	SEEK ERROR	RNF	RNF	0	RNF	0
S3	CRC ERROR	CRC ERROR	CRC ERROR	0	CRC ERROR	0
S2	TRACK 0	LOST DATA	LOST DATA	LOST DATA	LOST DATA	LOST DATA
S1	INDEX PULSE	DRQ	DRQ	DRQ	DRQ	DRQ
S0	BUSY	BUSY	BUSY	BUSY	BUSY	BUSY

### STATUS FOR TYPE I COMMANDS

BIT NAME	MEANING
S7 NOT READY	This bit when set indicates the drive is not ready. When reset it indicates that the drive is ready. This bit is an inverted copy of the Ready input and logically 'ored' with MR.
S6 PROTECTED	When set, indicates Write Protect is activated. This bit is an inverted copy of WRPT input.
S5 HEAD LOADED	When set, it indicates the head is loaded and engaged. This bit is a logical "and" of HLD and HLT signals.
S4 SEEK ERROR	When set, the desired track was not verified. This bit is reset to 0 when updated.
S3 CRC ERROR	CRC encountered in ID field.
S2 TRACK 00	When set, indicates Read/Write head is positioned to Track 0. This bit is an inverted copy of the TROO input.
S1 INDEX	When set, indicates index mark detected from drive. This bit is an inverted copy of the IP input.
S0 BUSY	When set command is in progress. When reset no command is in progress.

### STATUS FOR TYPE II AND III COMMANDS

BIT NAME	MEANING
S7 NOT READY	This bit when set indicates the drive is not ready. When reset, it indicates that the drive is ready. This bit is an inverted copy of the Ready input and 'ored' with MR. The Type II and III Commands will not execute unless the drive is ready.
S6 WRITE PROTECT	On Read Record: Not Used. On Read Track: Not Used. On any Write: It indicates a Write Protect. This bit is reset when updated.
S5 RECORD TYPE/ WRITE FAULT	On Read Record: It indicates the record-type code from data field address mark. 1 = Deleted Data Mark. 0 = Data Mark. On any Write: It indicates a Write Fault. This bit is reset when updated.
S4 RECORD NOT FOUND (RNF)	When set, it indicates that the desired track, sector, or side were not found. This bit is reset when updated.
S3 CRC ERROR	If S4 is set, an error is found in one or more ID fields; otherwise it indicates error in data field. This bit is reset when updated.
S2 LOST DATA	When set, it indicates the computer did not respond to DRQ in one byte time. This bit is reset to zero when updated.
S1 DATA REQUEST	This bit is a copy of the DRQ output. When set, it indicates the DR is full on a Read Operation or the DR is empty on a Write operation. This bit is reset to zero when updated.
S0 BUSY	When set, command is under execution. When reset, no command is under execution.





```

00000000 4A J4 LD C,A
00000001 00 J4 LD A,(HL)
00000002 00 J4 LD A,C
00000003 00 J4 CALL NZ,80B8
00000004 00 J4 LD NZ,8090
00000005 00 J4 LD A,50
00000006 00 J4 LD A,50
00000007 00 J4 LD NZ,80A3
00000008 00 J4 LD A,5B
00000009 00 J4 PUSH AF
00000010 00 J4 LD HL,0120
00000011 00 J4 LD DE,0014
00000012 00 J4 CALL 03B5
00000013 00 J4 POP AF
00000014 00 J4 LD NZ,80B4
00000015 00 J4 LD A,08
00000016 00 J4 POP HL
00000017 00 J4 POP DE
00000018 00 J4 POP BC
00000019 00 J4 RET
00000020 00 J4 CP 81
00000021 00 J4 RET C
00000022 00 J4 CP 78
00000023 00 J4 RET NC
00000024 00 J4 AND DF
00000025 00 J4 RET
00000026 00 J4 LD HL,0120
00000027 00 J4 LD DE,0030
00000028 00 J4 CALL 03B5
00000029 00 J4 POP BC
00000030 00 J4 POP DE
00000031 00 J4 POP HL
00000032 00 J4 RET
00000033 00 J4 PUSH HL
00000034 00 J4 PUSH DE
00000035 00 J4 LD C,A
00000036 00 J4 PUSH BC
00000037 00 J4 CP 07
00000038 00 J4 LD NZ,80C1
00000039 00 J4 LD A,02
00000040 00 J4 CALL 1501
00000041 00 J4 POP BC
00000042 00 J4 PUSH BC
00000043 00 J4 LD A,09
00000044 00 J4 LD (5080),A
00000045 00 J4 LD A,C
00000046 00 J4 AND 74
00000047 00 J4 CP 03
00000048 00 J4 LD NZ,80F1
00000049 00 J4 LD A,20
00000050 00 J4 RST 10
00000051 00 J4 LD A,03
00000052 00 J4 RST 10
00000053 00 J4 LD A,08
00000054 00 J4 RST 10
00000055 00 J4 POP BC
00000056 00 J4 POP DE
00000057 00 J4 POP HL
00000058 00 J4 RET
00000059 00 J4 LD A,(50B6)
00000060 00 J4 CP 74
00000061 00 J4 RET NZ
00000062 00 J4 LD HL,50B6
00000063 00 J4 LD DE,5036
00000064 00 J4 LD BC,3A
00000065 00 J4 LD C,(HL)
00000066 00 J4 LD A,(DE)
00000067 00 J4 LD (HL),A
00000068 00 J4 LD A,C
00000069 00 J4 LD (DE),A
00000070 00 J4 INC HL
00000071 00 J4 INC DE
00000072 00 J4 DJNZ 0104
00000073 00 J4 RET
00000074 00 J4 CALL 00F8
00000075 00 J4 LD SP,(8510)
00000076 00 J4 LD HL,(851E)
00000077 00 J4 LD BC,(500F)
00000078 00 J4 JP HL
00000079 00 J4 LD HL,8520 → INICIO SCRATCH?
00000080 00 J4 LD A,20
00000081 00 J4 LD B,20
00000082 00 J4 LD (HL),A
00000083 00 J4 INC HL
00000084 00 J4 DJNZ 0124
00000085 00 J4 LD (HL),00
00000086 00 J4 RET

```

BORRA 32 BYTES





00000000	00C80	PUSH	HL
00000000	00C80	CALL	0000
00000000	00000	POP	HL
00000000	00000	POP	HL
00000000	00100	JP	NZ, 0309
00000000	00000	OP	NO
00000000	00500	JP	NZ, 0325
00000000	00500	LD	A, A
00000000	00477	LD	A, (851A)
00000000	003A1	OR	10
00000000	00A10	JP	NZ, 03A2
00000000	00000	LD	A, C
00000000	00000	LD	(HL), A
00000000	00000	HZ	HL
00000000	00000	PUSH	HL
00000000	00600	CALL	HL
00000000	00600	POP	HL
00000000	00A10	LD	A, (851A)
00000000	00000	INC	A
00000000	00000	LD	(851A), A
00000000	001A85	LD	00FF
00000000	00000	LD	A, (851A)
00000000	00000	OR	A
00000000	00000	JP	NZ, 0321
00000000	00000	DEC	A
00000000	00000	LD	(851A), A
00000000	00000	DEC	HL
00000000	00000	LD	A, 20
00000000	00000	LD	(HL), A
00000000	00000	PUSH	HL
00000000	0012100	LD	HL, 0321 "
00000000	00000	CALL	0351
00000000	00000	POP	HL
00000000	00000	LD	HL, 03A2
00000000	00000	EX	AF, AF
00000000	00000	JP	NZ, 032C
00000000	00000	NOP	
00000000	00000	LD	A, 20
00000000	00000	JP	0000
00000000	00000	LD	A, (DE)
00000000	00000	CP	(HL)
00000000	00000	JP	NZ, 0334
00000000	00000	INC	DE
00000000	00000	INC	HL
00000000	00000	CUNZ	032A
00000000	00000	XOR	A
00000000	00000	RET	
00000000	00000	LD	A, FF
00000000	00000	OR	A
00000000	00000	RET	
00000000	1100000	LD	DE, 0000
00000000	00000	LD	B, 02
00000000	0214400	LD	HL, 0344 "
00000000	00000	LD	A, FF
00000000	00000	LD	(600E), A
00000000	00000	CALL	035C
00000000	00000	CALL	036C
00000000	00000	CALL	036C
00000000	00000	CALL	036C
00000000	00000	JP	0160





A0000	0000	LD	HL, 0000
A0001	0000	ADD	HL, 30
A0002	0000	LD	(R030), HL
A0003	0000	LD	SP, 0000
A0004	0000	LD	HL, 0000
A0005	0000	LD	(R030), HL
A0006	0000	LD	A, (501E)
A0007	0000	RND	00
A0008	0000	JR	N, R110
A0009	0000	LD	HL, 0004
A0010	0000	CALL	R478
A0011	0000	CALL	R005
A0012	0000	JP	R451
A0013	0000		
A0014	0000		
A0015	0000		
A0016	0000		
A0017	0000		
A0018	0000		
A0019	0000		
A0020	0000		
A0021	0000		
A0022	0000		
A0023	0000		
A0024	0000		
A0025	0000		
A0026	0000		
A0027	0000		
A0028	0000		
A0029	0000		
A0030	0000		
A0031	0000		
A0032	0000		
A0033	0000		
A0034	0000		
A0035	0000		
A0036	0000		
A0037	0000		
A0038	0000		
A0039	0000		
A0040	0000		
A0041	0000		
A0042	0000		
A0043	0000		
A0044	0000		
A0045	0000		
A0046	0000		
A0047	0000		
A0048	0000		
A0049	0000		
A0050	0000		
A0051	0000		
A0052	0000		
A0053	0000		
A0054	0000		
A0055	0000		
A0056	0000		
A0057	0000		
A0058	0000		
A0059	0000		
A0060	0000		
A0061	0000		
A0062	0000		
A0063	0000		
A0064	0000		
A0065	0000		
A0066	0000		
A0067	0000		
A0068	0000		
A0069	0000		
A0070	0000		
A0071	0000		
A0072	0000		
A0073	0000		
A0074	0000		
A0075	0000		
A0076	0000		
A0077	0000		
A0078	0000		
A0079	0000		
A0080	0000		
A0081	0000		
A0082	0000		
A0083	0000		
A0084	0000		
A0085	0000		
A0086	0000		
A0087	0000		
A0088	0000		
A0089	0000		
A0090	0000		
A0091	0000		
A0092	0000		
A0093	0000		
A0094	0000		
A0095	0000		
A0096	0000		
A0097	0000		
A0098	0000		
A0099	0000		
A0100	0000		





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A111E 00E9A4 CALL A4F9
A111F 00E9A4 LD A,0000
A1120 00E9A4 CALL A009
A1121 00E9A4 LD HL,A767
A1122 00E9A4 CALL A478
A1123 00E9A4 LD A,308
A1124 00E9A4 CALL A009
A1125 00E9A4 LD A,(A875)
A1126 00E9A4 OR 10
A1127 00E9A4 OUT (FF),A
A1128 00E9A4 LD (A875),A
A1129 00E9A4 XOR A
A1130 00E9A4 LD (A879),A
A1131 00E9A4 CALL A24A
A1132 00E9A4 LD A,(A878)
A1133 00E9A4 CP 31
A1134 00E9A4 JP NZ,A439
A1135 00E9A4 CP 32
A1136 00E9A4 JP NZ,A439
A1137 00E9A4 LD HL,A767
A1138 00E9A4 CALL A478
A1139 00E9A4 LD A,31
A1140 00E9A4 CALL A009
A1141 00E9A4 LD A,(A875)
A1142 00E9A4 AND EF
A1143 00E9A4 LD (A875),A
A1144 00E9A4 OUT (FF),A
A1145 00E9A4 CALL A24A
A1146 00E9A4 JP A439
A1147 00E9A4 CALL A000
A1148 00E9A4 XOR A
A1149 00E9A4 LD (A87C),A
A1150 00E9A4 LD A,09
A1151 00E9A4 PUSH AF
A1152 00E9A4 CALL A463
A1153 00E9A4 POP AF
A1154 00E9A4 INC A
A1155 00E9A4 CP OF
A1156 00E9A4 JR NZ,A253
A1157 00E9A4 LD D,00
A1158 00E9A4 LD A,(A876)
A1159 00E9A4 CP 56
A1160 00E9A4 JP NZ,A384
A1161 00E9A4 LD B,(A875)
A1162 00E9A4 AND F7
A1163 00E9A4 OUT (FF),A
A1164 00E9A4 LD A,FF
A1165 00E9A4 LD (A874),A
A1166 00E9A4 LD A,(A876)
A1167 00E9A4 CP 56
A1168 00E9A4 JP NZ,A384
A1169 00E9A4 LD DE,01
A1170 00E9A4 PUSH DE
A1171 00E9A4 LD HL,A772
A1172 00E9A4 CALL A478
A1173 00E9A4 POP DE
A1174 00E9A4 PUSH DE
A1175 00E9A4 LD C,D
A1176 00E9A4 LD B,00
A1177 00E9A4 CALL A11B
A1178 00E9A4 CALL A009
A1179 00E9A4 POP DE
A1180 00E9A4 LD HL,A9FC
A1181 00E9A4 LD B,0F
A1182 00E9A4 LD (HL),FF
A1183 00E9A4 INC HL
A1184 00E9A4 DJNZ A297
A1185 00E9A4 LD B,0B
A1186 00E9A4 LD (HL),00
A1187 00E9A4 INC HL
A1188 00E9A4 DJNZ A29E
A1189 00E9A4 LD (HL),FE
A1190 00E9A4 INC HL
A1191 00E9A4 LD (HL),D
A1192 00E9A4 INC HL
A1193 00E9A4 LD (HL),00
A1194 00E9A4 INC HL
A1195 00E9A4 PUSH DE
A1196 00E9A4 PUSH H
A1197 00E9A4 LD D,00
A1198 00E9A4 LD HL,A368
A1199 00E9A4 ADD HL,DE
A1200 00E9A4 LD E,(HL)
A1201 00E9A4 POP HL
A1202 00E9A4 LD (HL),E
A1203 00E9A4 POP DE
A1204 00E9A4 INC HL
A1205 00E9A4 LD (HL),01
A1206 00E9A4 INC HL
A1207 00E9A4 LD (HL),F7
A1208 00E9A4 INC HL
A1209 00E9A4 LD B,0B
A1210 00E9A4 LD (HL),FF
A1211 00E9A4 INC HL
A1212 00E9A4 DJNZ A2C0

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D00000 LD B,06
D00001 LD (HL),00
D00002 INC HL
D00003 DJNZ A207
D00004 LD (HL),FB
D00005 INC HL
D00006 LD DE,FF
D00007 PUSH DE
D00008 LD D,D
D00009 LD D,A2DF
D0000A LD (HL),E6
D0000B INC HL
D0000C DJNZ A206
D0000D LD (HL),E6
D0000E LD A,A207
D0000F LD (HL),FF
D00010 INC HL
D00011 DJNZ A2E0
D00012 LD (HL),FF
D00013 POP DE
D00014 INC HL
D00015 LD (HL),F7
D00016 INC HL
D00017 LD B,0B
D00018 LD (HL),FF
D00019 INC HL
D0001A DJNZ A2EE
D0001B INC HL
D0001C LD DE,E
D0001D CP DE
D0001E JP NZ,A29C
D0001F LD B,FF
D00020 LD (HL),FF
D00021 INC HL
D00022 DJNZ A2FC
D00023 DJNZ A2FC
D00024 PUSH DE
D00025 LD DE,0A
D00026 LD HL,A9FC
D00027 LD A,F4
D00028 OUT (1F),A
D00029 LD A,(A874)
D0002A OR A
D0002B JR NZ,A326
D0002C XOR A
D0002D LD (A874),A
D0002E LD B,05
D0002F LD A,FF
D00030 CALL A392
D00031 DJNZ A313
D00032 LD A,(A875)
D00033 OR A
D00034 OUT (FF),A
D00035 IN A,(FF)
D00036 AND C0
D00037 JR NZ,A326
D00038 JP A336
D00039 LD A,(HL)
D0003A OUT (7F),A
D0003B INC HL
D0003C JP A326
D0003D IN A,(1F)
D0003E AND 84
D0003F JR NZ,A340
D00040 AND 00
D00041 JR NZ,A34A
D00042 LD HL,A7D2
D00043 CALL A47B
D00044 EI
D00045 JP A1D4
D00046 DEC D
D00047 JR NZ,A305
D00048 POP DE
D00049 IN A,(3F)
D0004A OR A
D0004B PUSH DE
D0004C JR NZ,A363
D0004D LD DE,0A
D0004E LD A,09
D0004F OUT (5F),A
D00050 LD A,A0
D00051 LD HL,A897
D00052 DI
D00053 PUSH DE
D00054 CALL A386
D00055 POP DE
D00056 OUT (1F),A
D00057 IN A,(FF)
D00058 AND C0
D00059 JR NZ,A367
D0005A JP A378

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A370 7E LD A, (HL)
A371 00 CPL
A372 03 INC HL
A373 037F OUT (7F), A
A374 037A3 JP A357
A375 037B FEI
A376 037C 037F IN A, (1F)
A377 037D E63C AND 3C
A378 037E 04 JR NZ, A383
A379 037F 10 DEC E
A380 0380 035A3 JP NZ, A35A
A381 0381 01 POP
A382 0382 1E01 LD DE, 01
A383 0383 05 PUSH DE
A384 0384 0184A7 LD HL, A784
A385 0385 007BA4 CALL A47B
A386 0386 05 POP
A387 0387 4A PUSH DE
A388 0388 0000 LD CC, 0
A389 0389 0000 LD BC, 00
A390 0390 00181A CALL A18
A391 0391 0020 LD A, 20
A392 0392 0009A0 CALL A009
A393 0393 01 LD 0, 01
A394 0394 7A LD A, 7A
A395 0395 1E0A LD E, 0A
A396 0396 0357 OUT (57), A
A397 0397 0300 LD A, 30
A398 0398 0333 DI
A399 0399 05 PUSH DE
A400 03A0 0086A5 CALL A586
A401 03A1 01 POP
A402 03A2 001F OUT (1F), A
A403 03A3 0077 IN A, (77)
A404 03A4 0E6C AND C
A405 03A5 7A7A JR NZ, A3A6
A406 03A6 0B7FA3 JP M, A3B9
A407 03A7 037FA3 IN A, (7F)
A408 03A8 7B JP A3A8
A409 03A9 031F FEI
A410 03AA 0E6C AND 3C
A411 03AB 0354 JR NZ, A414
A412 03AC 10 DEC E
A413 03AD 002A1A3 JP NZ, A3A1
A414 03AE 0610 AND 10
A415 03AF 00196A7 LD HL, A796
A416 03B0 0000 JR NZ, A307
A417 03B1 0000 AND 00
A418 03B2 001A7A7 LD HL, A7AA
A419 03B3 0005 JR NZ, A307
A420 03B4 0604 AND 04
A421 03B5 0218A7 LD HL, A78E
A422 03B6 007BA4 CALL A47B
A423 03B7 00179A3 LD HL, A879
A424 03B8 0044 INC (HL)
A425 03B9 001E7A7 LD HL, A7EE
A426 03BA 007BA4 CALL A47B
A427 03BB 00037FA4 IN A, (3F)
A428 03BC 0600 LD B, 00
A429 03BD 4F LD C, A
A430 03BE 00181A CALL A18
A431 03BF 0020 LD A, 20
A432 03C0 0009A0 CALL A009
A433 03C1 0017FA7 LD HL, A7FF
A434 03C2 007BA4 CALL A47B
A435 03C3 0057 IN A, (5F)
A436 03C4 0600 LD B, 00
A437 03C5 4F LD C, A
A438 03C6 00181A CALL A18
A439 03C7 0020 LD A, 20
A440 03C8 0009A0 CALL A009
A441 03C9 0009A0 LD A, 09
A442 03CA 0009A0 CALL A009
A443 03CB 0009A0 LD A, 09
A444 03CC 0009A0 CALL A009
A445 03CD 0009A0 LD A, 09
A446 03CE 0009A0 CALL A009
A447 03CF 02D4A1 JP NZ, A1D4
A448 03D0 14 INC D
A449 03D1 7A LD A, D
A44A 03D2 7E0B CP B
A44B 03D3 039CA3 JP NZ, A39C
A44C 03D4 01 POP
A44D 03D5 14 INC DE
A44E 03D6 03A77A3 LD A, (A877)
A44F 03D7 00 SUB
A450 03D8 00 RET
A451 03D9 03E14 LD A, 14
A452 03DA 0009A0 CALL A009
A453 03DB 7A LD A, D
A454 03DC 037F OUT (7F), A
A455 03DD 03E18 LD A, 18
A456 03DE 031F OUT (1F), A
A457 03DF 0071A5 CALL A571
A458 03E0 03E18 LD A, 18
A459 03E1 0009A0 CALL A009
A460 03E2 037CA3 JP A273

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P4439 2107A8 LD HL,A807
P443F CD78A4 CALL A47B
P4440 3A79A8 LD A,(A879)
P4444 0600 LD B,00
P4445 4F LD C,A
P4448 CD181A CALL 1A18
P4449 2108A8 LD HL,A808
P444E CD78A4 CALL A47B
P4451 0004A1 JP A104
P4452 F8 EI
P4454 3EFF LD A,FF
P4454 D0FC OUT (FC),A
P4456 3E02 LD A,02
P4458 CD1016 CALL 1610
P445B 00680D CALL 0068
P445E ED7B85A8 LD SP,(A885)
P4463 F8 RET
P4464 3E16 LD A,16
P4468 CD09A0 CALL A009
P4469 F1 POP AF
P446A CD09A0 CALL A009
P446D AF XOR A
P446E CD09A0 CALL A009
P4471 0520 LD B,20
P4473 3E20 LD A,20
P4475 CD09A0 CALL A009
P4478 10F9 CJNZ A473
P447A 09 RET
P447B 7E LD A,(HL)
P447C B7 OR A
P447D C8 RET Z
P447E F8 PUSH HL
P447F CD09A0 CALL A009
P4482 E1 POP HL
P4483 23 INC HL
P4484 18F5 JR A47B
P4486 2183A8 LD HL,A883
P4489 0600 LD B,0A
P448B 3620 LD (HL),20
P448D 23 INC HL
P448E 18FB CJNZ A48B
P4490 2183A8 LD HL,A883
P4493 AF XOR A
P4494 3287A8 LD (A887),A
P4497 E8 PUSH HL
P4498 CD06A0 CALL A006
P449B FE20 CP 20
P449D 2879 JR Z,A498
P449F 1804 JR A4A5
P44A1 E8 PUSH HL
P44A2 CD06A0 CALL A006
P44A5 E1 POP HL
P44A6 FE08 CP 08
P44A8 281E JR Z,A4C8
P44AA FE00 CP 00
P44AC 08E4A4 JP Z,A4E4
P44AF 4F LD C,A
P44B0 3A87A8 LD A,(A887)
P44B3 FE08 CP 08
P44B5 288A JR Z,A4A1
P44B7 79 LD A,C
P44B8 77 LD (HL),A
P44B9 23 INC HL
P44BA F8 PUSH HL
P44BB CD09A0 CALL A009
P44BE E1 POP HL
P44BF 3A87A8 LD A,(A887)
P44C2 3C INC A
P44C3 3287A8 LD (A887),A
P44C6 1809 JR A4A1
P44C8 3A87A8 LD A,(A887)
P44CB B7 OR A
P44CC 28C2 JR Z,A490
P44CE 3D DEC A
P44CF 3287A8 LD (A887),A
P44D2 28B HL DEC HL
P44D3 3E20 LD A,20
P44D5 77 LD (HL),A
P44D8 E8 PUSH HL
P44D9 21E0A4 LD HL,A4E0
P44DA CD78A4 CALL A47B
P44DD E1 POP HL
P44DE 13C1 JR A4B1
P44E0 08 EX AF,AF
P44E1 2808 JR NZ,A4EB
P44E3 08 NOP
P44E4 3E20 LD A,20
P44E6 CD09A0 JP A009
P44E8 2197A8 LD HL,A897
P44EA 010001 LD BC,0100
P44EF 3600 LD (HL),00
P44F1 23 INC HL
P44F2 08 DEC BC
P44F3 79 LD A,C

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P44F B0 OR B
P44F 3007 JRN NZ, A4EF
P44F 327E LD A, 0A
P44F 3001 LD (A87E), A
P44F 3279 LD A, 01
P501 3001 LD (A879), A
P501 1880 LD HL, 0180
P501 4478 LD A, (A870)
P501 7FE31 CP 31
P501 330E JRN NZ, A519
P501 1116 LD HL, 0316
P501 3302 CP 20
P501 3307 JRN NZ, A519
P501 3303 JRN NZ, A519
P501 1440 JRN NZ, A519
P501 1360 LD HL, 0838
P501 2270 LD (A870), HL
P501 217A LD HL, A87A
P501 3519 LD (HL), 19
P501 7FE31 CP 31
P501 3518 JRN NZ, A533
P501 7FE30 LD (HL), 18
P501 3517 CP 32
P501 3517 JRN NZ, A533
P501 7FE33 LD (HL), 17
P501 3515 CP 33
P501 3515 JRN NZ, A533
P501 3515 LD (HL), 16
P501 3515 CALL A53A
P501 3515 CALL A54F
P501 3515 RET
P501 2115 LD HL, A815
P501 3515 CALL A47B
P501 3515 CALL A488
P501 2183 LD HL, A888
P501 1181 LD DE, A881
P501 0109 LD BC, 0009
P501 0009 LDIR
P501 0124 LD HL, A824
P501 3515 CALL A47B
P501 3515 CALL A488
P501 2183 LD HL, A888
P501 1181 LD DE, A881
P501 0109 LD BC, 0009
P501 0009 LDIR
P501 0009 RET
P501 117F LD DE, A87F
P501 2A70 LD HL, (A870)
P501 19 ADD HL, DE
P501 7FE XOR A
P501 7FE LD (HL), A
P501 3FE LD A, 0B
P501 031F OUT (1F), A
P501 08FF IN A, (FF)
P501 7FE AND 00
P501 7FE JRN NZ, A571
P501 7FE RET
P501 7FE LD A, C
P501 3070 LD (A870), A
P501 3FE LD A, FC
P501 81 OR C
P501 4F LD C, A
P501 117F LD DE, A87F
P501 2A70 LD HL, (A870)
P501 19 ADD HL, DE
P501 7FE LD A, (HL)
P501 030F OUT (3F), A
P501 7FE LD A, C
P501 03FF OUT (FF), A
P501 3275 LD (A875), A
P501 3275 LD A, 23
P501 8FE LD C, FF
P501 00 DEC C
P501 20FD JRN NZ, A594
P501 00 DEC A
P501 00FD JRN NZ, A592
P501 00FD RET
P501 4F LD C, A
P501 117F LD DE, A87F
P501 2A70 LD HL, (A870)
P501 19 ADD HL, DE
P501 7FE LD A, (HL)
P501 8FE POP C
P501 00 RET
P501 71 LD (HL), C
P501 79 LD A, C
P501 037F OUT (7F), A
P501 3E18 LD A, 18
P501 031F OUT (1F), A
P501 0071 CALL A571
P501 3E18 LD A, 10
P501 0392 LD A, 92
P501 57 XOR A
P501 7A XOR A
P501 09 LD A, 0
P501 09 RET

```

I

SCOPY

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000000 00000000 JP 00005
000001 00000000 JP 00000
000002 00000000 LD A, (5000)
000003 00000000 CP A, 4
000004 00000000 RET Z
000005 00000000 LD HL, 5000
000006 00000000 LD DE, 5000
000007 00000000 LD B, 3A
000008 00000000 LD C, (HL)
000009 00000000 LD A, (DE)
000010 00000000 LD (HL), A
000011 00000000 LD A, C
000012 00000000 LD (DE), A
000013 00000000 INC HL
000014 00000000 INC DE
000015 00000000 DJNZ 0014
000016 00000000 RET
000017 00000000 LD A, FF
000018 00000000 LD (5015), A
000019 00000000 XOR A
000020 00000000 LD (50F7), A
000021 00000000 CALL 00008
000022 00000000 LD A, AA
000023 00000000 LD (5017), A
000024 00000000 LD HL, 0097
000025 00000000 LD (501A), HL
000026 00000000 LD HL, 0000
000027 00000000 ADD HL, SP
000028 00000000 LD (SAFE), HL
000029 00000000 DEC HL
000030 00000000 DEC HL
000031 00000000 LD SP, HL
000032 00000000 CALL 00005
000033 00000000 CALL 00001
000034 00000000 LD HL, (505D)
000035 00000000 CALL 00005
000036 00000000 JP NZ, 0080
000037 00000000 CP A, 00
000038 00000000 INC HL
000039 00000000 JR NZ, 0040
000040 00000000 CALL 00005
000041 00000000 JR NZ, 0040
000042 00000000 CP A, 00
000043 00000000 JP NZ, 0080
000044 00000000 INC HL
000045 00000000 LD A, (HL)
000046 00000000 LD (5011), HL
000047 00000000 JP 0130
000048 00000000 LD A, (HL)
000049 00000000 CP 00
000050 00000000 RET NZ
000051 00000000 CP 00
000052 00000000 RET NZ
000053 00000000 CP A
000054 00000000 RET
000055 00000000 RET
000056 00000000 PUSH BC
000057 00000000 PUSH DE
000058 00000000 PUSH HL
000059 00000000 LD HL, 0A35
000060 00000000 CALL 000AF
000061 00000000 LD A, (5008)
000062 00000000 AND DF
000063 00000000 POP HL
000064 00000000 POP DE
000065 00000000 POP BC
000066 00000000 RET
000067 00000000 CALL 00006
000068 00000000 CALL 0004F
000069 00000000 CALL 00006
000070 00000000 LD SP, (SAFE)
000071 00000000 LD HL, (501A)
000072 00000000 LD BC, (500F)
000073 00000000 LD B, 00
000074 00000000 JP HL
000075 00000000 CALL 00004
000076 00000000 BIT 7, (IV+00)
000077 00000000 RET NZ
000078 00000000 LD HL, (5053)
000079 00000000 LD (5055), HL
000080 00000000 PUSH HL
000081 00000000 LD HL, 5092
000082 00000000 LD (5058), HL
000083 00000000 POP HL
000084 00000000 LD DE, 0A13
000085 00000000 LD SP, (503D)
000086 00000000 PUSH DE
000087 00000000 RET
000088 00000000 CALL 0009F
000089 00000000 CP 00
000090 00000000 RET Z

```

00000000	00	CALL	00055
00000000	00	JR	00055
00000000	00	LD	HL, (503D)
00000000	00	LD	(5013), HL
00000000	00	LD	HL, 8019
00000000	00	LD	(5030), HL
00000000	00	LD	HL, 8990
00000000	00	LD	(8019), HL
00000000	00	RET	
00000000	00	LD	HL, (5013)
00000000	00	LD	(5030), HL
00000000	00	RET	
00000000	00	LD	A, (5019)
00000000	00	JR	00055
00000000	00	XOR	A
00000000	00	LD	(50F7), A
00000000	00	LD	(500F), A
00000000	00	LD	HL, 8000
00000000	00	ADD	HL, SP
00000000	00	LD	(SAFE), HL
00000000	00	DEC	HL
00000000	00	DEC	HL
00000000	00	LD	SP, HL
00000000	00	CALL	000C1
00000000	00	LD	HL, 5017
00000000	00	LD	(HL), AA
00000000	00	LD	HL, FFFF
00000000	00	LD	(50FA), HL
00000000	00	LD	(50A8), HL
00000000	00	CALL	000A0
00000000	00	CALL	00098
00000000	00	CALL	00195
00000000	00	CALL	00073
00000000	00	CALL	00068
00000000	00	LD	HL, (SAFE)
00000000	00	DEC	HL
00000000	00	DEC	HL
00000000	00	LD	SP, HL
00000000	00	CALL	00065
00000000	00	CALL	00055
00000000	00	XOR	A
00000000	00	LD	(5015), A
00000000	00	LD	HL, 8112
00000000	00	LD	(501A), HL
00000000	00	CALL	000D8
00000000	00	CALL	000D8
00000000	00	XOR	A
00000000	00	LD	(500F), A
00000000	00	LD	HL, (5059)
00000000	00	LD	(5011), HL
00000000	00	LD	A, (HL)
00000000	00	CP	00
00000000	00	JR	NZ, 8103
00000000	00	LD	HL, 8AE3
00000000	00	LD	(HL), 00
00000000	00	HLD	C
00000000	00	LD	A, 00
00000000	00	CP	A, C
00000000	00	JR	ZC, 8000
00000000	00	LD	A, D
00000000	00	HLD	C
00000000	00	LD	HL, D
00000000	00	CP	(HL)
00000000	00	JR	NZ, 8142
00000000	00	XOR	A
00000000	00	LD	(500F), A
00000000	00	LD	(5006), A
00000000	00	LD	(5018), A
00000000	00	LD	HL, 503B
00000000	00	DEC	(HL)
00000000	00	LD	B, 00
00000000	00	LD	HL, 8AEC
00000000	00	DEC	C
00000000	00	HLAD	C
00000000	00	LD	HL, BC
00000000	00	LD	(HL)
00000000	00	HLD	C
00000000	00	LD	D, (HL)
00000000	00	EX	DE, HL
00000000	00	PUSH	HL
00000000	00	LD	DE, 8171
00000000	00	PUSH	DE
00000000	00	LD	HL, 503B
00000000	00	SET	(HL)
00000000	00	POP	HL
00000000	00	JP	HL





```

002A00 CDF182 CALL 02F1
002A01 CD6181A CALL 0AB1
002A02 CD6181A CALL 0AB1
002A03 ED45098D LD BC, (8D00)
002A04 CD6E8888 CALL 888E
002A05 02130888 LD HL, 883C
002A06 CD7388A CALL 8A73
002A07 C3808888 JP 8080
002A08 320F8D LD (5D0F), A
002A09 32158D LD A, (5D15)
002A0A B7 OR D
002A0B CC738A CALL Z, 8A73
002A0C C9 RET
002A0D 210088 LD HL, 8B00
002A0E 3E01 LD A, 01
002A0F C3AB887 JP 878B
002A10 CD0D883 CALL 830D
002A11 7E LD A, (HL)
002A12 B7 OR D
002A13 CAA382 JP Z, 82A3
002A14 FE01 CP 01
002A15 C0C883 CALL Z, 83C8
002A16 C0 RET NZ
002A17 18F0 JR 82CF
002A18 AF XOR A
002A19 320C5C LD (50CC), A
002A1A ED550C5C LD DE, (50CC)
002A1B 1500 LD D, 00
002A1C 211B8C LD HL, 8C1B
002A1D 0601 LD B, 01
002A1E C3093C JP 3C09
002A1F 110800 LD DE, 0008
002A20 18F3 JR 82E9
002A21 CDF182 CALL 82F1
002A22 3A028D LD A, (8D02)
002A23 FE07 CP 07
002A24 280C JR Z, 830C
002A25 FE0A CP 0A
002A26 2808 JR Z, 830C
002A27 21F78B LD HL, 8BF7
002A28 CD738A CALL 8A73
002A29 18A0 JR 82E9
002A2A ED4BF65C LD BC, (8CF6)
002A2B 21045C LD HL, 5CC4
002A2C 89 ADD HL, BC
002A2D 77 LD (HL), A
002A2E 3AFE8C LD A, (8CFE)
002A2F 23 INC HL
002A30 23 INC HL
002A31 23 INC HL
002A32 23 INC HL
002A33 77 LD (HL), A
002A34 21065D LD HL, 5D06
002A35 11056D LD DE, 8D05
002A36 0509 LD B, 09
002A37 C0B68A CALL 8AB6
002A38 C8 RET Z
002A39 C05F82 CALL 825F
002A3A 18EF JR 831D
002A3B 8A115D LD HL, (5D11)
002A3C 23 INC HL
002A3D 7E LD A, (HL)
002A3E FE00 CP 00
002A3F CA4583 JP Z, 8345
002A40 CDF488 CALL 88F4
002A41 C08788 CALL 8887
002A42 C0C388 CALL 88C3
002A43 EB EX DE, HL
002A44 C0ED87 CALL 87ED
002A45 C08788 CALL 8887
002A46 CDF588 CALL 82F6
002A47 C0AC88 CALL 88AC
002A48 C09B88 CALL 889B
002A49 21068C LD HL, 8C06
002A4A CD738A CALL 8A73
002A4B 21108D LD HL, 8D10
002A4C CD738A CALL 8A73
002A4D C0B18A CALL 8AB1
002A4E 3AFF8C LD A, (8CFF)
002A4F 210F8D LD HL, 8D0F
002A50 95 SUB (HL)
002A51 E5 PUSH HL
002A52 C0DE8A CALL 8ADE
002A53 210888 LD HL, 8B03
002A54 C0738A CALL 8A73
002A55 E1 POP HL
002A56 4E LD C, (HL)
002A57 C00F8A CALL 8ADF
002A58 210C8B LD HL, 8B0C
002A59 CD738A CALL 8A73
002A5A C0CF82 CALL 82CF
002A5B 211B8C LD HL, 8C1B
002A5C C0CF82 CALL 82CF
002A5D C0B18A CALL 8AB1

```





```

CP      55
JR      NZ,85
LD      D,NZ,(5CF1)
OR      D,NZ
JC      B
LD      NZ,8584
LD      D,A,(5CF1)
XOR      A,A
LD      D,(5CF1),A
PUSH      B
LD      D,(5CCE),A
LD      D,A,(5CF8)
LD      D,A
CALL      3096
LD      HL,802E
PUSH      HL
LD      DE,(5CF2)
CALL      3099
LD      HL,(5CF4)
LD      D,(5CF2),HL
CALL      88AC
LD      HL,8889
CALL      8A73
CALL      886E
CP      59
JR      NZ,8580
LD      D,A,(8C18)
OR      A,A
CALL      NZ,84C1
POP      HL
POP      BC
LD      DE,(5CEB)
LD      D,A
LD      D,(5CCE),A
CALL      3090
LD      HL,(5CF4)
LD      D,(5CEB),HL
JR      359F
LD      D,(5CF1),A
LD      B,60
XOR      A,A
JR      353B
LD      B,43
LD      D,A,(5C06)
CP      81
JR      NZ,85AC
LD      D,A,(5D10)
OR      D,D
JR      NZ,85AC
CALL      389F
CP      DE
LD      B,43
JR      NN,85AC
CP      4
LD      B,44
JR      NN,85AC
LD      B,42
LD      HL,5CE5
LD      D,(HL),B
BT
CALL      88F4
CALL      8887
CALL      8580
CALL      37E2
JP      NZ,8207
PUSH      BC
CALL      82F1
LD      D,A,(80FF)
POP      BC
INZ      C
CP      00
JR      NZ,85D1
DEC      A
LD      D,(80FF),A
XOR      A,A
PUSH      AF
JR      NZ,85D8
LD      HL,8D6F
INC      HL
PUSH      HL
CALL      8883
POP      BC
DEC      C
CALL      8614
POP      AF
JP      NZ,85E7
LD      D,A,81
LD      D,(5CDD),A
PUSH      AF
CALL      862C

```

```

355FE F1 POP AF
355FF0 C0200000 JPB NZ,0000
355FF2 C00F1000 CALL 02F1
355FF4 00000000 LD HL,(5CEB)
355FF6 00270000 LD (0CF0),HL
355FF8 00000000 LD DE,(5CEA)
355FFA 00000000 LD HL,(0000)
35600 10000000 LD D,00
35604 10000000 ADD HL,DE
35608 00000000 LD (0000),HL
3560C 00000000 JPB 0000
35610 00140000 CALL 0614
35614 00000000 LD A,(5C00)
35618 00000000 CP 01
3561C 00000000 RET
35620 00000000 XOR A
35624 00000000 PUSH BC
35628 00000000 CALL 075B
3562C 00000000 POP BC
35630 00000000 RET
35634 00000000 LD A,FF
35638 00000000 JR 0615
3563C 00000000 LD HL,(5C61)
35640 00000000 LD (5CCF),HL
35644 00100000 LD BC,1000
35648 00000000 CALL 095A
3564C 00000000 RET
35650 00180000 CALL 061B
35654 00000000 JPB 0000
35658 00000000 LD (5CD7),HL
3565C 00000000 LD (5CDB),HL
35660 00000000 LD DE,(5CEA)
35664 00000000 LD HL,(5CD9)
35668 10000000 LD D,00
3566C 10000000 ADD HL,DE
35670 00000000 LD (5CD9),HL
35674 00000000 RET
35678 00000000 CALL 0807
3567C 00000000 CALL 02F6
35680 00000000 LD A,(0D0F)
35684 00000000 OR A
35688 00000000 JPB NZ,0000
3568C 00100000 LD HL,0000
35690 00000000 LD (5CD9),HL
35694 00000000 LD C,FF
35698 00000000 INC C
3569C 00000000 CALL 060B
356A0 00000000 JPB NZ,065B
356A4 00000000 LD A,C
356A8 00000000 LD (5CD4),A
356AC 00000000 LD HL,(5CEB)
356B0 00000000 CALL 0532
356B4 00000000 INC C
356B8 00000000 CALL 060B
356BC 00000000 JPB NZ,066B
356C0 00000000 CP 00
356C4 00000000 JPB NZ,068D
356C8 00000000 LD A,(5CD4)
356CC 00000000 LD C,A
356D0 00000000 INC C
356D4 00000000 CALL 060B
356D8 00000000 CP 00
356DC 00000000 JPB NZ,06E9
356E0 00000000 XOR A
356E4 00000000 LD (5CDD),A
356E8 00000000 CALL 062C
356EC 00000000 CALL 0632
356F0 00000000 JPB 0670
356F4 00000000 LD A,(5CEA)
356F8 00000000 LD (5CD3),A
35704 00000000 LD (5CD1),A
35708 00000000 LD HL,(5CEB)
3570C 00000000 LD (5CD5),HL
35710 00000000 PUSH BC
35714 00000000 CALL 071C
35718 00000000 POP BC
3571C 00000000 LD HL,(5CF4)
35720 00000000 LD (5CD5),HL
35724 00000000 LD (5CEB),HL
35728 00000000 XOR A
3572C 00000000 LD (5CEA),A
35730 00000000 LD A,(5CDD)
35734 00000000 PUSH AF
35738 00000000 LD A,01
3573C 00000000 LD (5CDD),A
35740 00000000 CALL 062C
35744 00000000 POP AF
35748 00000000 LD (5CDD),A
35754 00000000 LD A,(5CD4)
35758 00000000 LD C,A
3575C 00000000 LD HL,(5CDB)
35760 00000000 LD (5CEB),HL
35764 00000000 LD A,(5CD1)
35768 00000000 LD (5CEA),A
3576C 00000000 CALL 062C

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0601 3AD45C LD A, (5CD4)
0604 3C INC A
0605 4F LD C, A
0606 CD1485 CALL 3614
0609 2A055C LD HL, (5CD5)
060C 22E85C LD (5CEB), HL
060F CD2C85 CALL 362C
0612 3AD45C LD A, (5CD4)
0615 4F LD C, A
0618 C35838 JP 3658
0619 2A075C LD HL, (5CCF)
061C CDFF182 CALL 32F1
061F 2A008D LD HL, (3D00)
0622 ED58095C LD DE, (5CD9)
0625 19 ADD HL, DE
0628 22008D LD (3D00), HL
062B 3AFF78C LD A, (3CFF)
062E 010F8D LD HL, 300F
0631 98 SUB (HL)
0634 32FF8C LD (3CFF), A
0637 3500 LD (HL), 00
063A 2AD55C LD HL, (5CD5)
063D 127C8C LD (3CFC), HL
0640 75 PUSH AF
0643 CD8389 CALL 3983
0646 71 POP AF
0649 4F LD C, A
064C CD1485 CALL 3614
064F 7F XOR A
0652 32D05C LD (5CD0), A
0655 033C84 JP 343C
0658 3AD35C LD A, (5CD3)
065B 87 OR A
065E 28 RET NZ
0661 D660 SUB 60
0664 302E JR NC, 8753
0667 3AD35C LD A, (5CD3)
066A 47 LD B, A
066D 7F XOR A
0670 32D35C LD (5CD3), A
0673 C5 PUSH BC
0676 32CE5C LD (5CCE), A
0679 212E8D LD HL, 8D2E
067C E5 PUSH HL
067F ED58D55C LD DE, (5CD5)
0682 CD09300 CALL 3C09
0685 2AF45C LD HL, (5CF4)
0688 22D55C LD (5CD5), HL
068B 71 POP HL
068E C1 POP BC
0691 ED58D075C LD DE, (5CD7)
0694 CD0C300 CALL 3C0C
0697 2AF45C LD HL, (5CF4)
069A 22D75C LD (5CD7), HL
069D 75118C9 JR 871C
06A0 32D35C LD (5CD3), A
06A3 0660 LD B, 60
06A6 7F XOR A
06A9 72D JR 872D
06AC 75B F5 PUSH AF
06AF 210C5C LD HL, 5C0C
06B2 3500 LD (HL), 00
06B5 79 LD A, C
06B8 C510 SUB 10
06BB 3503 JR C, 8769
06BE 34 INC (HL)
06C1 18F9 JR 8762
06C4 C510 ADD A, 10
06C7 4F LD C, A
06CA C5 PUSH BC
06CD CD8382 CALL 3983
06D0 71 POP BC
06D3 71 POP AF
06D6 CD1888 CALL 3618
06D9 110D5C LD DE, 5C0D
06DC 011000 LD BC, 0010
06DF B7 OR A
06E2 3501 JR Z, 877F
06E5 EB EX DE, HL
06E8 ED80 LD IR
06EB RET
06EE EB EX DE, HL
06F1 37 SCF
06F4 ED52 SBC HL, DE
06F7 D8 RET C
06FA 110A00 LD DE, 000A
06FD 19 ADD HL, DE
0700 44 LD B, H
0703 4D LD C, L
0706 21051F LD HL, 1F05
0709 CD8F88 CALL 368F
070C C9 RET

```



```

00000000 J0 LD A,C
00000001 J1 DCP NZ,8841
00000002 J2 DCP BC
00000003 J3 DCP 00
00000004 J4 DCP 00
00000005 J5 DCP 00
00000006 J6 DCP 00
00000007 J7 DCP 00
00000008 J8 DCP 00
00000009 J9 DCP 00
0000000A J0 DCP 00
0000000B J1 DCP 00
0000000C J2 DCP 00
0000000D J3 DCP 00
0000000E J4 DCP 00
0000000F J5 DCP 00
00000010 J6 DCP 00
00000011 J7 DCP 00
00000012 J8 DCP 00
00000013 J9 DCP 00
00000014 J0 DCP 00
00000015 J1 DCP 00
00000016 J2 DCP 00
00000017 J3 DCP 00
00000018 J4 DCP 00
00000019 J5 DCP 00
0000001A J6 DCP 00
0000001B J7 DCP 00
0000001C J8 DCP 00
0000001D J9 DCP 00
0000001E J0 DCP 00
0000001F J1 DCP 00
00000020 J2 DCP 00
00000021 J3 DCP 00
00000022 J4 DCP 00
00000023 J5 DCP 00
00000024 J6 DCP 00
00000025 J7 DCP 00
00000026 J8 DCP 00
00000027 J9 DCP 00
00000028 J0 DCP 00
00000029 J1 DCP 00
0000002A J2 DCP 00
0000002B J3 DCP 00
0000002C J4 DCP 00
0000002D J5 DCP 00
0000002E J6 DCP 00
0000002F J7 DCP 00
00000030 J8 DCP 00
00000031 J9 DCP 00
00000032 J0 DCP 00
00000033 J1 DCP 00
00000034 J2 DCP 00
00000035 J3 DCP 00
00000036 J4 DCP 00
00000037 J5 DCP 00
00000038 J6 DCP 00
00000039 J7 DCP 00
0000003A J8 DCP 00
0000003B J9 DCP 00
0000003C J0 DCP 00
0000003D J1 DCP 00
0000003E J2 DCP 00
0000003F J3 DCP 00
00000040 J4 DCP 00
00000041 J5 DCP 00
00000042 J6 DCP 00
00000043 J7 DCP 00
00000044 J8 DCP 00
00000045 J9 DCP 00
00000046 J0 DCP 00
00000047 J1 DCP 00
00000048 J2 DCP 00
00000049 J3 DCP 00
0000004A J4 DCP 00
0000004B J5 DCP 00
0000004C J6 DCP 00
0000004D J7 DCP 00
0000004E J8 DCP 00
0000004F J9 DCP 00
00000050 J0 DCP 00
00000051 J1 DCP 00
00000052 J2 DCP 00
00000053 J3 DCP 00
00000054 J4 DCP 00
00000055 J5 DCP 00
00000056 J6 DCP 00
00000057 J7 DCP 00
00000058 J8 DCP 00
00000059 J9 DCP 00
0000005A J0 DCP 00
0000005B J1 DCP 00
0000005C J2 DCP 00
0000005D J3 DCP 00
0000005E J4 DCP 00
0000005F J5 DCP 00
00000060 J6 DCP 00
00000061 J7 DCP 00
00000062 J8 DCP 00
00000063 J9 DCP 00
00000064 J0 DCP 00
00000065 J1 DCP 00
00000066 J2 DCP 00
00000067 J3 DCP 00
00000068 J4 DCP 00
00000069 J5 DCP 00
0000006A J6 DCP 00
0000006B J7 DCP 00
0000006C J8 DCP 00
0000006D J9 DCP 00
0000006E J0 DCP 00
0000006F J1 DCP 00
00000070 J2 DCP 00
00000071 J3 DCP 00
00000072 J4 DCP 00
00000073 J5 DCP 00
00000074 J6 DCP 00
00000075 J7 DCP 00
00000076 J8 DCP 00
00000077 J9 DCP 00
00000078 J0 DCP 00
00000079 J1 DCP 00
0000007A J2 DCP 00
0000007B J3 DCP 00
0000007C J4 DCP 00
0000007D J5 DCP 00
0000007E J6 DCP 00
0000007F J7 DCP 00
00000080 J8 DCP 00
00000081 J9 DCP 00
00000082 J0 DCP 00
00000083 J1 DCP 00
00000084 J2 DCP 00
00000085 J3 DCP 00
00000086 J4 DCP 00
00000087 J5 DCP 00
00000088 J6 DCP 00
00000089 J7 DCP 00
0000008A J8 DCP 00
0000008B J9 DCP 00
0000008C J0 DCP 00
0000008D J1 DCP 00
0000008E J2 DCP 00
0000008F J3 DCP 00
00000090 J4 DCP 00
00000091 J5 DCP 00
00000092 J6 DCP 00
00000093 J7 DCP 00
00000094 J8 DCP 00
00000095 J9 DCP 00
00000096 J0 DCP 00
00000097 J1 DCP 00
00000098 J2 DCP 00
00000099 J3 DCP 00
0000009A J4 DCP 00
0000009B J5 DCP 00
0000009C J6 DCP 00
0000009D J7 DCP 00
0000009E J8 DCP 00
0000009F J9 DCP 00
000000A0 J0 DCP 00
000000A1 J1 DCP 00
000000A2 J2 DCP 00
000000A3 J3 DCP 00
000000A4 J4 DCP 00
000000A5 J5 DCP 00
000000A6 J6 DCP 00
000000A7 J7 DCP 00
000000A8 J8 DCP 00
000000A9 J9 DCP 00
000000AA J0 DCP 00
000000AB J1 DCP 00
000000AC J2 DCP 00
000000AD J3 DCP 00
000000AE J4 DCP 00
000000AF J5 DCP 00
000000B0 J6 DCP 00
000000B1 J7 DCP 00
000000B2 J8 DCP 00
000000B3 J9 DCP 00
000000B4 J0 DCP 00
000000B5 J1 DCP 00
000000B6 J2 DCP 00
000000B7 J3 DCP 00
000000B8 J4 DCP 00
000000B9 J5 DCP 00
000000BA J6 DCP 00
000000BB J7 DCP 00
000000BC J8 DCP 00
000000BD J9 DCP 00
000000BE J0 DCP 00
000000BF J1 DCP 00
000000C0 J2 DCP 00
000000C1 J3 DCP 00
000000C2 J4 DCP 00
000000C3 J5 DCP 00
000000C4 J6 DCP 00
000000C5 J7 DCP 00
000000C6 J8 DCP 00
000000C7 J9 DCP 00
000000C8 J0 DCP 00
000000C9 J1 DCP 00
000000CA J2 DCP 00
000000CB J3 DCP 00
000000CC J4 DCP 00
000000CD J5 DCP 00
000000CE J6 DCP 00
000000CF J7 DCP 00
000000D0 J8 DCP 00
000000D1 J9 DCP 00
000000D2 J0 DCP 00
000000D3 J1 DCP 00
000000D4 J2 DCP 00
000000D5 J3 DCP 00
000000D6 J4 DCP 00
000000D7 J5 DCP 00
000000D8 J6 DCP 00
000000D9 J7 DCP 00
000000DA J8 DCP 00
000000DB J9 DCP 00
000000DC J0 DCP 00
000000DD J1 DCP 00
000000DE J2 DCP 00
000000DF J3 DCP 00
000000E0 J4 DCP 00
000000E1 J5 DCP 00
000000E2 J6 DCP 00
000000E3 J7 DCP 00
000000E4 J8 DCP 00
000000E5 J9 DCP 00
000000E6 J0 DCP 00
000000E7 J1 DCP 00
000000E8 J2 DCP 00
000000E9 J3 DCP 00
000000EA J4 DCP 00
000000EB J5 DCP 00
000000EC J6 DCP 00
000000ED J7 DCP 00
000000EE J8 DCP 00
000000EF J9 DCP 00
000000F0 J0 DCP 00
000000F1 J1 DCP 00
000000F2 J2 DCP 00
000000F3 J3 DCP 00
000000F4 J4 DCP 00
000000F5 J5 DCP 00
000000F6 J6 DCP 00
000000F7 J7 DCP 00
000000F8 J8 DCP 00
000000F9 J9 DCP 00
000000FA J0 DCP 00
000000FB J1 DCP 00
000000FC J2 DCP 00
000000FD J3 DCP 00
000000FE J4 DCP 00
000000FF J5 DCP 00

```



```

00000000 00000000 CALL 0000
00000000 00000000 JR NZ,0000
00000000 00000000 CALL 0000
00000000 00000000 LD (0007),BC
00000000 00000000 CALL 0000
00000000 00000000 CP NZ,0000
00000000 00000000 JP NZ,0000
00000000 00000000 CALL 0000
00000000 00000000 JR NZ,0000
00000000 00000000 CALL 0000
00000000 00000000 LD A,(0010)
00000000 00000000 OR A
00000000 00000000 LD (0009),BC
00000000 00000000 JR NZ,0000
00000000 00000000 LD HL,(0007)
00000000 00000000 ADD HL,BC
00000000 00000000 CDD (0009),HL
00000000 00000000 CP NZ,0000
00000000 00000000 JR NZ,0000
00000000 00000000 CALL 0000
00000000 00000000 LD HL,0000
00000000 00000000 LD (000B),HL
00000000 00000000 JR 004F
00000000 00000000 CALL 0000
00000000 00000000 RET NZ
00000000 00000000 CALL 0000
00000000 00000000 LD (000B),BC
00000000 00000000 LD HL,(0011)
00000000 00000000 LD (0002),HL
00000000 00000000 LD HL,11A7
00000000 00000000 JR 005B
00000000 00000000 LD HL,(0051)
00000000 00000000 LD (0002),HL
00000000 00000000 LD HL,0030
00000000 00000000 JR 005B
00000000 00000000 LD (0002),HL
00000000 00000000 LD HL,0020
00000000 00000000 PUSH HL
00000000 00000000 LD HL,(0002)
00000000 00000000 CALL 00E5
00000000 00000000 RET
00000000 00000000 LD (0002),HL
00000000 00000000 LD HL,19E8
00000000 00000000 JR 005B
00000000 00000000 LD (0002),HL
00000000 00000000 LD HL,1655
00000000 00000000 JR 005B
00000000 00000000 LD DE,0045
00000000 00000000 DEC DE
00000000 00000000 LD B,01
00000000 00000000 LD HL,0C18
00000000 00000000 JP 0000
00000000 00000000 CALL 0000
00000000 00000000 JP 0000
00000000 00000000 JP 0000
00000000 00000000 LD HL,(00FE)
00000000 00000000 OR HL
00000000 00000000 LD HL,0000
00000000 00000000 CALL 0000
00000000 00000000 JP 0000
00000000 00000000 POP HL
00000000 00000000 POP HL
00000000 00000000 JP 0000
00000000 00000000 LD A,(0017)
00000000 00000000 CALL NZ,0000
00000000 00000000 CALL 0000
00000000 00000000 PUSH HL
00000000 00000000 JP 001E
00000000 00000000 LD HL,00CA
00000000 00000000 LD BC,005B
00000000 00000000 CALL 1555
00000000 00000000 LD A,74
00000000 00000000 LD (001E),A
00000000 00000000 LD A,00
00000000 00000000 LD (0019),A
00000000 00000000 LD A,00
00000000 00000000 LD (000A),A
00000000 00000000 RET
00000000 00000000 CALL 00A3
00000000 00000000 CALL 00A7
00000000 00000000 LD A,(0017)
00000000 00000000 CALL 0000
00000000 00000000 PUSH HL
00000000 00000000 JP 00E1

```

```

000E5 220250 LD (5D02),HL
000E6 ED53045D LD (5D04),DE
000E7 D1 POP DE
000E8 E1 POP HL
000E9 D5 PUSH DE
000EA CD138A CALL 8A13
000EB 11028A LD DE,8A02
000EC D5 PUSH DE
000ED D5 PUSH HL
000EE ED5B045D LD DE,(5D04)
000EF 2A025D LD HL,(5D02)
000F0 C9 RET
000F1 21138A LD HL,8A13
000F2 01 OI
000F3 F5 PUSH AF
000F4 CD278A CALL 8A27
000F5 3A165D LD A,(5D16)
000F6 E67F AND 7F
000F7 32165D LD (5D16),A
000F8 D3FF OUT (FF),A
000F9 F1 POP AF
000FA C9 RET
000FB F5 PUSH AF
000FC CD278A CALL 8A27
000FD 3A165D LD A,(5D16)
000FE F688 OR 88
000FF 32165D LD (5D16),A
00100 D3FF OUT (FF),A
00101 CD2D8A CALL 8A2D
00102 F1 POP AF
00103 FB RI
00104 C9 RET
00105 CD428A CALL 8A42
00106 D3FC OUT (FC),A
00107 C9 RET
00108 CD428A CALL 8A42
00109 F688 OR 88
0010A D3FC OUT (FC),A
0010B C9 RET
0010C 213B5C LD HL,5C3B
0010D 7E LD A,(HL)
0010E E620 AND 20
0010F 28FB JR NZ,8A38
00110 3E20 LD A,20
00111 AE XOR (HL)
00112 77 LD (HL),A
00113 C9 RET
00114 3A485C LD A,(5C48)
00115 E638 AND 38
00116 0F RRC A
00117 0F RRC A
00118 0F RRC A
00119 C9 RET
0011A CD278A CALL 8A27
0011B 3EFF LD A,FF
0011C D3FF OUT (FF),A
0011D C9 RET
0011E CD468A CALL 8A46
0011F LDDR
00120 18A3 JR 8A02
00121 CD468A CALL 8A46
00122 ED80 LD IR
00123 18A1 JR 8A02
00124 E5 PUSH HL
00125 D5 PUSH DE
00126 D5 PUSH BC
00127 E67F AND 7F
00128 CD5D8A CALL 8A5D
00129 C1 POP BC
0012A C1 POP DE
0012B E1 POP HL
0012C C9 RET
0012D 211000 LD HL,0010
0012E CD8F88 JP 888F
0012F 7E LD A,(HL)
00130 B7 OR A
00131 C8 RET NZ
00132 CD518A CALL 8A51
00133 0B7E BIT 7,(HL)
00134 C8 RET NZ
00135 23 INC HL
00136 13F4 JR 8A73
00137 2A595C LD HL,(5C59)
00138 3600 LD (HL),00
00139 225B5C LD (5C5B),HL
0013A 23 INC HL
0013B 3680 LD (HL),80
0013C C9 RET

```

3A088	3A0F5D	LD	A, (500F)
3A089	0B7	OR	A
3A090	0C07F0A	CALL	Z, 0A7F
3A091	0C08595C	LD	HL, (5059)
3A092	0C0813A	CALL	0A61
3A093	0C08195D	LD	AP, (5D19)
3A094	0C0841	ADD	A, 41
3A095	0C08618A	CALL	0A61
3A096	0C0823	LD	AP, 23
3A097	0C08618A	CALL	0A61
3A098	0C0813A5C	LD	HL, 5C3A
3A099	0C08777F	LD	(HL), 7F
3A100	0C08488	CALL	08A4
3A101	0C08988	CALL	08B9
3A102		RET	
3A103	03E00	LD	A, 00
3A104	03E18A	JP	0A61
3A105	11	LD	A, (DE)
3A106	0BE	CP	(HL)
3A107	0206	JR	NZ, 0AC0
3A108	13	INC	DE
3A109	103	INC	HL
3A110	107F0	JNZ	0AB6
3A111	077F0	XOR	A
3A112	009	RET	
3A113	070FF	OR	FF
3A114	0055	RET	
3A115	0C55	PUSH	BC
3A116	03E00	LD	B, 00
3A117	03E00	LD	AP, (HL)
3A118	0C0818A	CALL	0A61
3A119	020	INC	HL
3A120	107F0	JNZ	0AC6
3A121	03E30	LD	A, 30
3A122	0C0818A	CALL	0A61
3A123	07E	LD	A, (HL)
3A124	0C0818A	CALL	0A61
3A125	03E00	LD	AP, 00
3A126	0C0818A	CALL	0A61
3A127	000108A	CALL	0A61
3A128	00000	POP	BC
3A129	00000	RET	
3A130	0277	CPL	
3A131	047	LD	C, A
3A132	0600	LD	B, 00
3A133	03E00	JP	08BE

0000	0000	0000	0000
0001	0000	0000	0000
0002	0000	0000	0000
0003	0000	0000	0000
0004	0000	0000	0000
0005	0000	0000	0000
0006	0000	0000	0000
0007	0000	0000	0000
0008	0000	0000	0000
0009	0000	0000	0000
0010	0000	0000	0000
0011	0000	0000	0000
0012	0000	0000	0000
0013	0000	0000	0000
0014	0000	0000	0000
0015	0000	0000	0000
0016	0000	0000	0000
0017	0000	0000	0000
0018	0000	0000	0000
0019	0000	0000	0000
0020	0000	0000	0000
0021	0000	0000	0000
0022	0000	0000	0000
0023	0000	0000	0000
0024	0000	0000	0000
0025	0000	0000	0000
0026	0000	0000	0000
0027	0000	0000	0000
0028	0000	0000	0000
0029	0000	0000	0000
0030	0000	0000	0000
0031	0000	0000	0000
0032	0000	0000	0000
0033	0000	0000	0000
0034	0000	0000	0000
0035	0000	0000	0000
0036	0000	0000	0000
0037	0000	0000	0000
0038	0000	0000	0000
0039	0000	0000	0000
0040	0000	0000	0000
0041	0000	0000	0000
0042	0000	0000	0000
0043	0000	0000	0000
0044	0000	0000	0000
0045	0000	0000	0000
0046	0000	0000	0000
0047	0000	0000	0000
0048	0000	0000	0000
0049	0000	0000	0000
0050	0000	0000	0000
0051	0000	0000	0000
0052	0000	0000	0000
0053	0000	0000	0000
0054	0000	0000	0000
0055	0000	0000	0000
0056	0000	0000	0000
0057	0000	0000	0000
0058	0000	0000	0000
0059	0000	0000	0000
0060	0000	0000	0000
0061	0000	0000	0000
0062	0000	0000	0000
0063	0000	0000	0000
0064	0000	0000	0000
0065	0000	0000	0000
0066	0000	0000	0000
0067	0000	0000	0000
0068	0000	0000	0000
0069	0000	0000	0000
0070	0000	0000	0000
0071	0000	0000	0000
0072	0000	0000	0000
0073	0000	0000	0000
0074	0000	0000	0000
0075	0000	0000	0000
0076	0000	0000	0000
0077	0000	0000	0000
0078	0000	0000	0000
0079	0000	0000	0000
0080	0000	0000	0000
0081	0000	0000	0000
0082	0000	0000	0000
0083	0000	0000	0000
0084	0000	0000	0000
0085	0000	0000	0000
0086	0000	0000	0000
0087	0000	0000	0000
0088	0000	0000	0000
0089	0000	0000	0000
0090	0000	0000	0000
0091	0000	0000	0000
0092	0000	0000	0000
0093	0000	0000	0000
0094	0000	0000	0000
0095	0000	0000	0000
0096	0000	0000	0000
0097	0000	0000	0000
0098	0000	0000	0000
0099	0000	0000	0000
0100	0000	0000	0000

J

1

DISC-CAT

```

10 CLEAR 59999
20 RANDOMIZE USR 15363: REM :
LOAD "disc-cat" CODE 624,512
30 INPUT "Nombre del fichero "
;n#
40 RANDOMIZE USR 624

```

```

EA69 2A4B5C LD HL,(5C4B)
EA6B 7E LLD A,(HL)
EA6D FE4E CP A,4E
EA6F 20010 JR NZ,EA78
EA71 000819 CALL 1983
EA73 EB EX DE,HL
EA75 8058595C LLD DE,(5C59)
EA77 A7 AND A
EA79 8052 HL,DE
EA7B EB EX DE,HL
EA7D 38ED JR C,EA83
EA7F 07 RST 0
EA81 004B4E LD HL,4B4E
EA83 23 INC HL
EA85 7E LLD A,(HL)
EA87 0001 OR A,1
EA89 0003 RET NZ
EA8B 7E INC HL
EA8D 00A1EB CALL EA81
EA8F 001AEB CALL EA1A
EA91 78 LD A,B
EA93 0001 OR A,1
EA95 2001B JR NZ,EA94
EA97 07 RST 0
EA99 00 DEFB 0

```

EA77 01 DEFB 01  
EA78 23 INC HL  
EA79 4E LD C,(HL)

```

EA9B 00 DEFB 0
EA9C 00 NOP
EA9E 70000000 RES 0,(IY+02)
EA9F 11930000 LD DE,EB93
EAA1 00E10000 CALL EAE1
EAA3 11E30000 LD DE,EA99
EAA5 00E10000 CALL EAE1
EAA7 80480000 LD BC,(EB93)
EAA9 002B0000 CALL BC,00
EAB1 00E30000 CALL BC,00
EAB3 117A0000 LD DE,EAFA
EAB5 00E10000 CALL EAE1
EAB7 80480000 LD BC,(EB95)
EAB9 002B0000 CALL BC,00
EABB 110A0000 LD DE,EB0A
EABD 00E10000 CALL EAE1
EABF 80480000 LD BC,(EB97)
EAC1 0000 LD B,00
EAC3 001B1A CALL 1A1B
EAC5 3E00 LD A,00
EAC7 07 RST 10
EAC9 09 RET
EAD1 1A LD A,(DE)
EAD3 13 INC DE
EAD5 7AFF CP A,F
EAD7 03 RET NZ
EAD9 07 RST 10
EADB 13FB JR EA81

```

EADE	00	00	44	04	00	43
EAE1	74	47	44	04	00	43
EAE3	77	00	44	04	00	43
EAE5	49	43	00	04	00	43
EAE7	77	00	44	04	00	43
EAE9	77	40	00	04	00	43
EAEB	77	4F	00	04	00	43
EAE5	77	3A	13	00	04	00

```

EB1A 3A175D LD A,(5D17)
EB1D FEAA CP AA
EB1F 04383C CALL NZ,3C38
EB22 CDAA3C CALL 3CAA
EB23 85 PUSH HL
EB26 00213D CALL 3D21
EB29 3E7F LD A,FF
EB2E 32155D LD (5D15),A
EB31 AF XOR A
EB34 32F75C LD (5CF7),A
EB38 CDAA63D CALL 3DA6
EB39 3EAA LD A,AA
EB3C 32175D LD (5D17),A
EB3E 017E01 LD HL,017E
EB40 221A5D LD (5D1A),HL
EB43 39 ADD HL,SP
EB44 22105D LD (5D10),HL
EB47 2B DEC HL
EB48 2B DEC HL
EB49 F9 LD SP,HL
EB4A CDAA901 CALL 01A8
EB4D C0C206 CALL 06C2
EB50 C04803 CALL 0348
EB53 11065D LD DE,5D06
EB56 21EA5B LD HL,5BEA
EB59 010900 LD BC,0009
EB5C ED80 LD IR
EB5E C05003 CALL 0350
EB61 AF XOR A
EB64 32065C LD (5CD6),A
EB67 3E43 LD A,43
EB6A 32AE55C LD (5CE5),A
EB6D C0C206 CALL 06C2
EB70 11005C LD DE,5C00
EB73 2198EB LD HL,EB98
EB76 010300 LD BC,0003
EB79 ED80 LD IR
EB7C C0383D CALL 3D38
EB7E C0E306 CALL 06E3
EB81 2AE63C LD HL,(5CE6)
EB84 2293EB LD (EB93),HL
EB87 2295EB LD (EB95),HL
EB8A 32EA5C LD A,(5CEA)
EB8D 3297EB LD (EB97),A
EB90 C36E01 JP 015E

```

```

EB93 60 EA 00 00 02 63 61 74
EB96 61 64 6F 72 20 7F 06 08

```

```

EBA1 0608 LD B,08
EBA3 1198EB LD DE,EB98
EBA6 EB EX DE,HL
EBA7 1A LD A,(DE)
EBA8 77 LD (HL),A
EBA9 23 INC HL
EBAE 13 INC DE
EBAF 00 DEC C
EBAE 2306 JR Z,EBB4
EBAE 10F7 DJNZ EBA7
EBB0 09 RET
EBB1 3620 LD (HL),20
EBB3 23 INC HL
EBB4 10FB DJNZ EBB1
EBB6 09 RET

```

(K)

# WESTERN DIGITAL

C O R P O R A T I O N

## FD179X-02

### Floppy Disk Formatter/Controller Family

**FEATURES**

- TWO VFO CONTROL SIGNALS — RG & VFOE
- SOFT SECTOR FORMAT COMPATIBILITY
- AUTOMATIC TRACK SEEK WITH VERIFICATION
- ACCOMMODATES SINGLE AND DOUBLE DENSITY FORMATS
  - IBM 3740 Single Density (FM)
  - IBM System 34 Double Density (MFM)
  - Non IBM Format for Increased Capacity
- READ MODE
  - Single/Multiple Sector Read with Automatic Search or Entire Track Read
  - Selectable 128, 256, 512 or 1024 Byte Sector Lengths
- WRITE MODE
  - Single/Multiple Sector Write with Automatic Sector Search
  - Entire Track Write for Diskette Formatting
- SYSTEM COMPATIBILITY
  - Double Buffering of Data 8 Bit Bi-Directional Bus for Data, Control and Status
  - DMA or Programmed Data Transfers
  - All Inputs and Outputs are TTL Compatible
  - On-Chip Track and Sector Registers/Comprehensive Status Information

**PROGRAMMABLE CONTROLS**

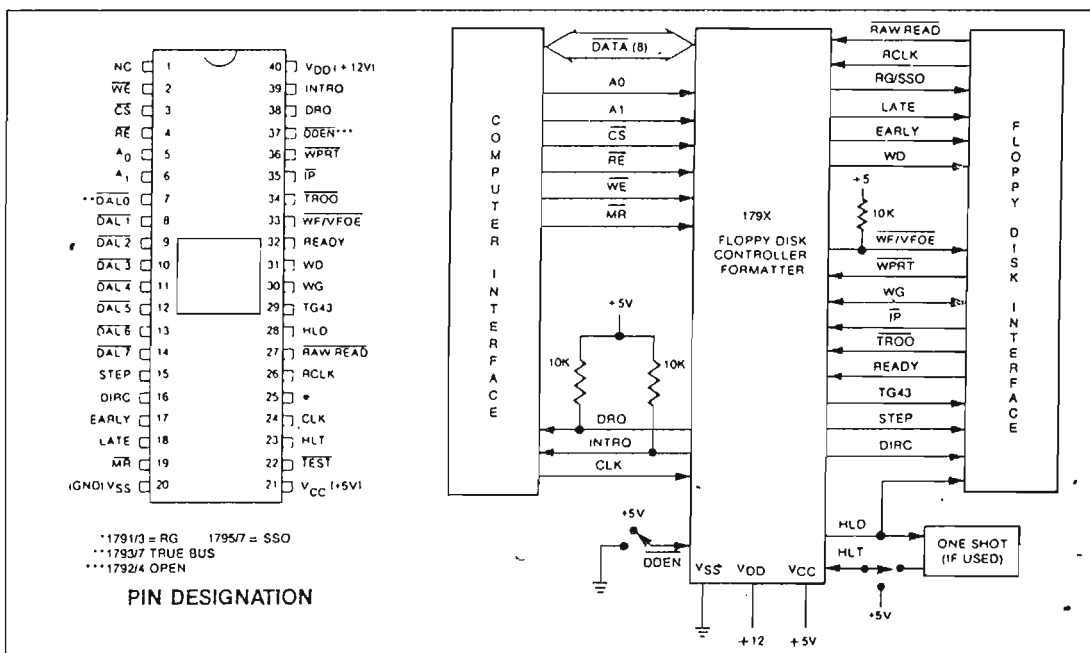
- Selectable Track to Track Stepping Time
- Side Select Compare
- INTERFACES TO WD1691 DATA SEPARATOR
- WINDOW EXTENSION
- INCORPORATES ENCODING/DECODING AND ADDRESS MARK CIRCUITRY
- FD1792/4 IS SINGLE DENSITY ONLY
- FD1795/7 HAS A SIDE SELECT OUTPUT

**179X-02 FAMILY CHARACTERISTICS**

FEATURES	1791	1792	1793	1794	1795	1797
Single Density (FM)	X	X	X	X	X	X
Double Density (MFM)	X		X		X	X
True Data Bus			X	X		X
Inverted Data Bus	X	X			X	
Write Precomp	X	X	X	X	X	X
Side Selection Output					X	X

**APPLICATIONS**

8" FLOPPY AND 5 1/4" MINI FLOPPY CONTROLLER  
SINGLE OR DOUBLE DENSITY  
CONTROLLER/FORMATTER



FD179X SYSTEM BLOCK DIAGRAM

PIN OUTS

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION																									
1	NO CONNECTION	NC	Pin 1 is internally connected to a back bias generator and must be left open by the user.																									
19	MASTER RESET	$\overline{MR}$	A logic low (50 microseconds min.) on this input resets the device and loads HEX 03 into the command register. The Not Ready (Status Bit 7) is reset during $\overline{MR}$ ACTIVE. When $\overline{MR}$ is brought to a logic high a RESTORE Command is executed, regardless of the state of the Ready signal from the drive. Also, HEX 01 is loaded into sector register.																									
20	POWER SUPPLIES	Vss	Ground																									
21		Vcc	+5V $\pm$ 5%																									
40		Voo	+12V $\pm$ 5%																									
COMPUTER INTERFACE:																												
2	WRITE ENABLE	$\overline{WE}$	A logic low on this input gates data on the DAL into the selected register when $\overline{CS}$ is low.																									
3	CHIP SELECT	$\overline{CS}$	A logic low on this input selects the chip and enables computer communication with the device.																									
4	READ ENABLE	$\overline{RE}$	A logic low on this input controls the placement of data from a selected register on the DAL when $\overline{CS}$ is low.																									
5,6	REGISTER SELECT LINES	A0, A1	These inputs select the register to receive/transfer data on the DAL lines under $\overline{RE}$ and $\overline{WE}$ control: <table border="1" style="margin-left: 20px;"> <thead> <tr> <th><math>\overline{CS}</math></th> <th>A1</th> <th>A0</th> <th><math>\overline{RE}</math></th> <th><math>\overline{WE}</math></th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>Status Reg</td> <td>Command Reg</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>Track Reg</td> <td>Track Reg</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>Sector Reg</td> <td>Sector Reg</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>Data Reg</td> <td>Data Reg</td> </tr> </tbody> </table>	$\overline{CS}$	A1	A0	$\overline{RE}$	$\overline{WE}$	0	0	0	Status Reg	Command Reg	0	0	1	Track Reg	Track Reg	0	1	0	Sector Reg	Sector Reg	0	1	1	Data Reg	Data Reg
$\overline{CS}$	A1	A0	$\overline{RE}$	$\overline{WE}$																								
0	0	0	Status Reg	Command Reg																								
0	0	1	Track Reg	Track Reg																								
0	1	0	Sector Reg	Sector Reg																								
0	1	1	Data Reg	Data Reg																								
7-14	DATA ACCESS LINES	DAL0-DAL7	Eight bit Bidirectional bus used for transfer of data, control, and status. This bus is receiver enabled by $\overline{WE}$ or transmitter enabled by $\overline{RE}$ . Each line will drive 1 standard TTL load.																									
24	CLOCK	CLK	This input requires a free-running 50% duty cycle square wave clock for internal timing reference, 2 MHz $\pm$ 1% for 8" drives, 1 MHz $\pm$ 1% for mini-floppies.																									
38	DATA REQUEST	DRQ	This open drain output indicates that the DR contains assembled data in Read operations, or the DR is empty in Write operations. This signal is reset when serviced by the computer through reading or loading the DR in Read or Write operations, respectively. Use 10K pull-up resistor to +5.																									
39	INTERRUPT REQUEST	INTRQ	This open drain output is set at the completion of any command and is reset when the STATUS register is read or the command register is written to. Use 10K pull-up resistor to +5.																									
FLOPPY DISK INTERFACE:																												
15	STEP	STEP	The step output contains a pulse for each step.																									
16	DIRECTION	DIRC	Direction Output is active high when stepping in, active low when stepping out.																									
17	EARLY	EARLY	Indicates that the WRITE DATA pulse occurring while Early is active (high) should be shifted early for write precompensation.																									
18	LATE	LATE	Indicates that the write data pulse occurring while Late is active (high) should be shifted late for write precompensation.																									
22	TEST	TEST	This input is used for testing purposes only and should be tied to +5V or left open by the user unless interfacing to voice coil actuated steppers.																									
23	HEAD LOAD TIMING	HLD	When a logic high is found on the HLD input the head is assumed to be engaged. It is typically derived from a 1 shot triggered by HLD.																									
25	READ GATE (1791, 1792, 1793, 1794)	RG	This output is used for synchronization of external data separators. The output goes high after two Bytes of zeros in single density, or 4 Bytes of either zeros or ones in double density operation.																									
25	SIDE SELECT OUTPUT (1795, 1797)	SSO	The logic level of the Side Select Output is directly controlled by the 'S' flag in Type II or III commands. When U = 1, SSO is set to a logic 1. When U = 0, SSO is set to a logic 0. The SSO is compared with the side information in the Sector I.D. Field. If they do not compare Status Bit 4 (RNF) is set. The Side Select Output is only updated at the beginning of a Type II or III command. It is forced to a logic 0 upon a MASTER RESET condition.																									
26	READ CLOCK	RCLK	A nominal square-wave clock signal derived from the data stream must be provided to this input. Phasing (i.e. RCLK transitions) relative to RAW READ is important but polarity (RCLK high or low) is not.																									
27	RAW READ	$\overline{RAW READ}$	The data input signal directly from the drive. This input shall be a negative pulse for each recorded flux transition.																									
28	HEAD LOAD	HLD	The HLD output controls the loading of the Read/Write head against the media.																									
29	TRACK GREATER THAN 43	TG43	This output informs the drive that the Read/Write head is positioned between tracks 44-76. This output is valid only during Read and Write Commands.																									
30	WRITE GATE	WG	This output is made valid before writing is to be performed on the diskette.																									
31	WRITE DATA	WD	A 200 ns (MFM) or 500 ns (FM) output pulse per flux transition. WD contains the unique Address marks as well as data and clock in both FM and MFM formats.																									
32	READY	READY	This input indicates disk readiness and is sampled for a logic high before Read or Write commands are performed. If Ready is low the Read or Write operation is not performed and an interrupt is generated. Type I operations are performed regardless of the state of Ready. The Ready input appears in inverted format as Status Register bit 7.																									

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
33	WRITE FAULT VFO ENABLE	WF/VFOE	This is a bi-directional signal used to signify writing faults at the drive, and to enable the external PLO data separator. When WG = 1, Pin 33 functions as a WF input. If WF = 0, any write command will immediately be terminated. When WG = 0, Pin 33 functions as a VFOE output. VFOE will go low during a read operation after the head has loaded and settled (HLT = 1). On the 1795/7, it will remain low until the last bit of the second CRC byte in the ID field. VFOE will then go high until 8 bytes (MFM) or 4 bytes (FM) before the Address Mark. It will then go active until the last bit of the second CRC byte of the Data Field. On the 1791/3, VFOE will remain low until the end of the Data Field. This pin has an internal 100K Ohm pull-up resistor.
34	TRACK 00	TROO	This input informs the FD179X that the Read/Write head is positioned over Track 00.
35	INDEX PULSE	IP	This input informs the FD179X when the index hole is encountered on the diskette.
36	WRITE PROTECT	WPRT	This input is sampled whenever a Write Command is received. A logic low terminates the command and sets the Write Protect Status bit.
37	DOUBLE DENSITY	DDEN	This input pin selects either single or double density operation. When DDEN = 0, double density is selected. When DDEN = 1, single density is selected. This line must be left open on the 1792/4.

**GENERAL DESCRIPTION**

The FD179X are N-Channel Silicon Gate MOS LSI devices which perform the functions of a Floppy Disk Formatter/Controller in a single chip implementation. The FD179X, which can be considered the end result of both the FD1771 and FD1781 designs, is IBM 3740 compatible in single density mode (FM) and System 34 compatible in Double Density Mode (MFM). The FD179X contains all the features of its predecessor the FD1771, plus the added features necessary to read/write and format a double density diskette. These include address mark detection, FM and MFM encode and decode logic, window extension, and write precompensation. In order to maintain compatibility, the FD1771, FD1781, and FD179X designs were made as close as possible with the computer interface, instruction set, and I/O registers being identical. Also, head load control is identical. In each case, the actual pin assignments vary by only a few pins from any one to another.

The processor interface consists of an 8-bit bi-directional bus for data, status, and control word transfers. The FD179X is set up to operate on a multiplexed bus with other bus-oriented devices.

The FD179X is TTL compatible on all inputs and outputs. The outputs will drive ONE TTL load or three LS loads. The 1793 is identical to the 1791 except the DAL lines are TRUE for systems that utilize true data busses.

The 1795/7 has a side select output for controlling double sided drives, and the 1792 and 1794 are "Single Density Only" versions of the 1791 and 1793 respectively. On these devices, DDEN must be left open.

**ORGANIZATION**

The Floppy Disk Formatter block diagram is illustrated on page 5. The primary sections include the parallel processor interface and the Floppy Disk interface.

**Data Shift Register** — This 8-bit register assembles serial data from the Read Data input (RAW READ) during Read operations and transfers serial data to the Write Data output during Write operations.

**Data Register** — This 8-bit register is used as a holding register during Disk Read and Write operations. In Disk Read operations the assembled data byte is transferred in parallel to the Data Register from the Data Shift Register. In Disk Write operations information is transferred in parallel from the Data Register to the Data Shift Register.

When executing the Seek command the Data Register holds the address of the desired Track position. This register is loaded from the DAL and gated onto the DAL under processor control.

**Track Register** — This 8-bit register holds the track number of the current Read/Write head position. It is incremented by one every time the head is stepped in (towards track 76) and decremented by one when the head is stepped out (towards track 00). The contents of the register are compared with the recorded track number in the ID field during disk Read, Write, and Verify operations. The Track Register can be loaded from or transferred to the DAL. This Register should not be loaded when the device is busy.

**Sector Register (SR)** — This 8-bit register holds the address of the desired sector position. The contents of the register are compared with the recorded sector number in the ID field during disk Read or Write operations. The Sector Register contents can be loaded from or transferred to the DAL. This register should not be loaded when the device is busy.

**Command Register (CR)** — This 8-bit register holds the command presently being executed. This register should not be loaded when the device is busy unless the new command is a force interrupt. The command register can be loaded from the DAL, but not read onto the DAL.

**Status Register (STR)** — This 8-bit register holds device Status information. The meaning of the Status bits is a function of the type of command previously executed. This register can be read onto the DAL, but not loaded from the DAL.

**CRC Logic** — This logic is used to check or to generate the 16-bit Cyclic Redundancy Check (CRC). The polynomial is:  $G(x) = x^{16} + x^{11} + x^4 + 1$ .

The CRC includes all information starting with the address mark and up to the CRC characters. The CRC register is preset to ones prior to data being shifted through the circuit.

**Arithmetic/Logic Unit (ALU)** — The ALU is a serial comparator, incrementer, and decrements and is used for register modification and comparisons with the disk recorded ID field.

**Timing and Control** — All computer and Floppy Disk interface controls are generated through this logic. The internal device timing is generated from an external crystal clock.

The FD179X has two different modes of operation according to the state of DDEN. When DDEN = 0 double density (MFM) is assumed. When DDEN = 1, single density (FM) is assumed. 1792 & 1794 are single density only.

**AM Detector** — The address mark detector detects ID, data and index address marks during read and write operations.

**PROCESSOR INTERFACE**

The interface to the processor is accomplished through the eight Data Access Lines (DAL) and associated control signals. The DAL are used to transfer Data, Status, and Control words out of, or into the FD179X. The DAL are three state buffers that are enabled as output drivers when Chip Select (CS) and Read Enable (RE) are active (low logic state) or act as input receivers when CS and Write Enable (WE) are active.

When transfer of data with the Floppy Disk Controller is required by the host processor, the device address is decoded and CS is made low. The address bits A1 and A0, combined with the signals RE during a Read operation or WE during a Write operation are interpreted as selecting the following registers:

A1	A0	READ (RE)	WRITE (WE)
0	0	Status Register	Command Register
0	1	Track Register	Track Register
1	0	Sector Register	Sector Register
1	1	Data Register	Data Register

During Direct Memory Access (DMA) types of data transfers between the Data Register of the FD179X and the processor, the Data Request (DRO) output is used in Data Transfer control. This signal also appears as status bit 1 during Read and Write operations.

On Disk Read operations the Data Request is activated (set high) when an assembled serial input byte is transferred in parallel to the Data Register. This bit is cleared when the Data Register is read by the processor. If the Data Register is read after one or more characters are lost, by having new data transferred into the register prior to processor readout, the Lost Data bit is set in the Status Register. The Read operation continues until the end of sector is reached.

On Disk Write operations the data Request is activated when the Data Register transfers its contents to the Data



Shift Register, and requires a new data byte. It is reset when the Data Register is loaded with new data by the processor. If new data is not loaded at the time the next serial byte is required by the Floppy Disk, a byte of zeroes is written on the diskette and the Lost Data bit is set in the Status Register.

At the completion of every command an INTRQ is generated. INTRQ is reset by either reading the status register or by loading the command register with a new command. In addition, INTRQ is generated if a Force Interrupt command condition is met.

The 179X has two modes of operation according to the state of DDEN (Pin 37). When DDEN = 1, single density is selected. In either case, the CLK input (Pin 24) is at 2 MHz. However, when interfacing with the mini-floppy, the CLK input is set at 1 MHz for both single density and double density.

**GENERAL DISK READ OPERATIONS**

Sector lengths of 128, 256, 512 or 1024 are obtainable in either FM or MFM formats. For FM, DDEN should be placed to logical "1." For MFM formats, DDEN should be placed to a logical "0." Sector lengths are determined at format time by the fourth byte in the "ID" field.

Sector Length Table*	
Sector Length Field (hex)	Number of Bytes in Sector (decimal)
00	128
01	256
02	512
03	1024

\*1795/97 may vary — see command summary.

The number of sectors per track as far as the FD179X is concerned can be from 1 to 255 sectors. The number of tracks as far as the FD179X is concerned is from 0 to 255 tracks. For IBM 3740 compatibility, sector lengths are 128 bytes with 26 sectors per track. For System 34 compatibility (MFM), sector lengths are 256 bytes/sector with 26 sectors/track; or lengths of 1024 bytes/sector with 8 sectors/track. (See Sector Length Table)

For read operations in 8\* double density the FD179X requires RAW READ Data (Pin 27) signal which is a 200 ns pulse per flux transition and a Read clock (RCLK) signal to indicate flux transition spacings. The RCLK (Pin 26) signal is provided by some drives but if not it may be derived externally by Phase lock loops, one shots, or counter techniques. In addition, a Read Gate Signal is provided as an output (Pin 25) on 1791/92/93/94 which can be used to inform phase lock loops when to acquire synchronization. When reading from the media in FM, RG is made true when 2 bytes of zeroes are detected. The FD179X must find an address mark within the next 10 bytes; otherwise RG is reset and the search for 2 bytes of zeroes begins all over again. If an address mark is found within 10 bytes, RG

remains true as long as the FD179X is deriving any useful information from the data stream. Similarly for MFM, RG is made active when 4 bytes of "00" or "FF" are detected. The FD179X must find an address mark within the next 16 bytes, otherwise RG is reset and search resumes.

During read operations (WG = 0), the VFOE (Pin 33) is provided for phase lock loop synchronization. VFOE will go active low when:

- a) Both HLT and HLD are True
- b) Settling Time, if programmed, has expired
- c) The 179X is inspecting data off the disk

If WF/VFOE is not used, leave open or tie to a 10K resistor to +5.

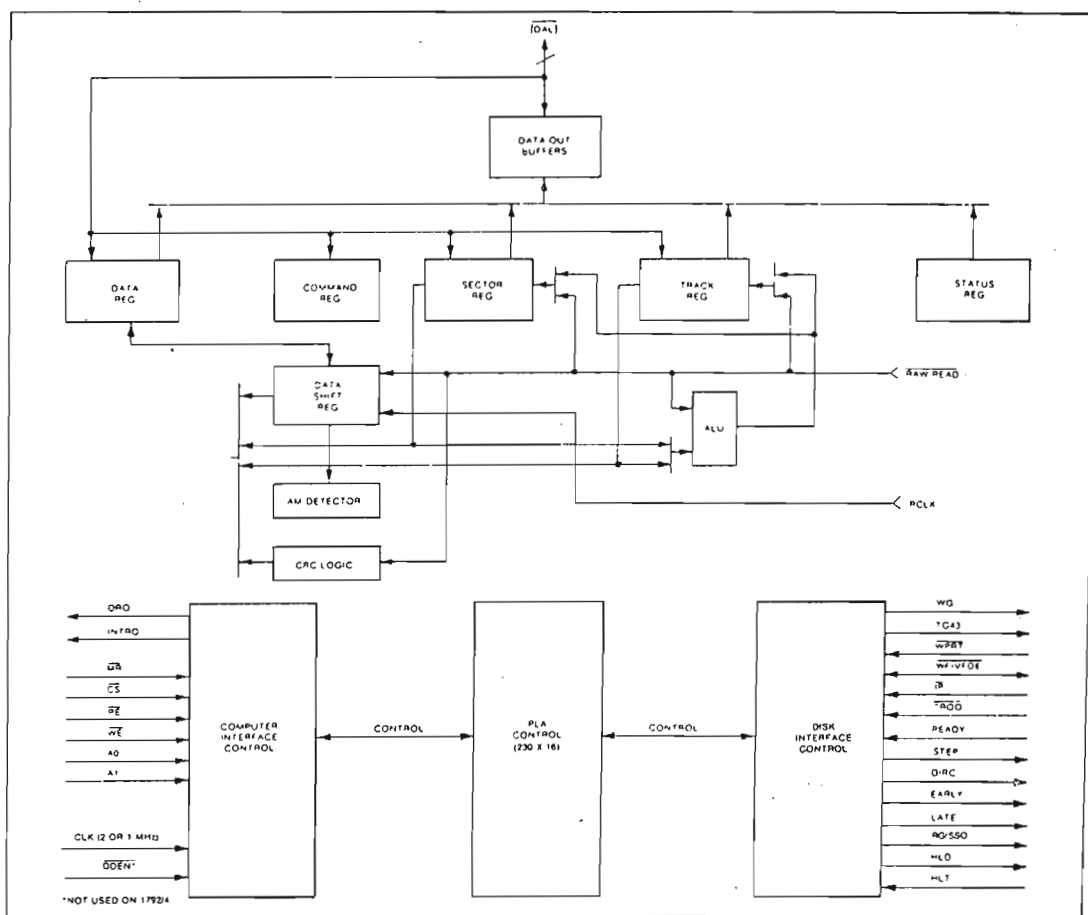
**GENERAL DISK WRITE OPERATION**

When writing is to take place on the diskette the Write Gate (WG) output is activated, allowing current to flow into the Read/Write head. As a precaution to erroneous writing the first data byte must be loaded into the Data Register in response to a Data Request from the FD179X before the Write Gate signal can be activated.

Writing is inhibited when the Write Protect input is a logic low, in which case any Write command is immediately terminated, an interrupt is generated and the Write Protect status bit is set. The Write Fault input, when activated, signifies a writing fault condition detected in disk drive electronics such as failure to detect write current flow when the Write Gate is activated. On detection of this fault the FD179X terminates the current command, and sets the Write Fault bit (bit 5) in the Status Word. The Write Fault input should be made inactive when the Write Gate output becomes inactive.

For write operations, the FD179X provides Write Gate (Pin 30) and Write Data (Pin 31) outputs. Write data consists of a series of 500 ns pulses in FM (DDEN = 1) and 200 ns pulses in MFM (DDEN = 0). Write Data provides the unique address marks in both formats.

Also during write, two additional signals are provided for write precompensation. These are EARLY (Pin 17) and LATE (Pin 18). EARLY is active true when the WD pulse appearing on (Pin 30) is to be written EARLY. LATE is active true when the WD pulse is to be written LATE. If both EARLY and LATE are low when the WD pulse is present, the WD pulse is to be written at nominal. Since write precompensation values vary from disk manufacturer to disk manufacturer, the actual value is determined by several one shots or delay lines which are located external to the FD179X. The write precompensation signals EARLY and LATE are valid for the duration of WD in both FM and MFM formats.



FD179X BLOCK DIAGRAM

**READY**

Whenever a Read or Write command (Type II or III) is received the FD179X samples the Ready input. If this input is logic low the command is not executed and an interrupt is generated. All Type I commands are performed regardless of the state of the Ready input. Also, whenever a Type II or III command is received, the TG43 signal output is updated.

**COMMAND DESCRIPTION**

The FD179X will accept eleven commands. Command words should only be loaded in the Command Register when the Busy status bit is off (Status bit 0). The one exception is the Force Interrupt command. Whenever a command is being executed, the Busy status bit is set. When a command is completed, an interrupt is generated and the Busy status bit is reset. The Status Register indicates whether the completed command encountered an error or was fault free. For ease of discussion, commands are divided into four types. Commands and types are summarized in Table 1.

**TABLE 1. COMMAND SUMMARY**

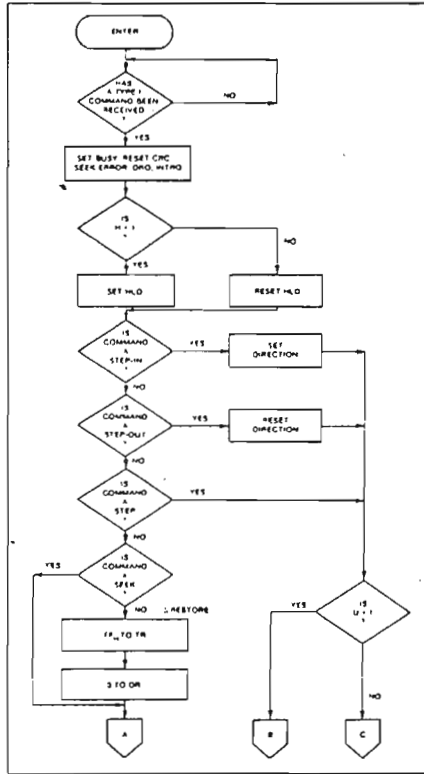
A. Commands for Models: 1791, 1792, 1793, 1794									B. Commands for Models: 1795, 1797								
Type	Command	7	6	5	Bits				7	6	5	Bits					
					4	3	2	1	0				4	3	2	1	0
I	Restore	0	0	0	0	h	V	r <sub>1</sub>	r <sub>0</sub>	0	0	0	0	h	V	r <sub>1</sub>	r <sub>0</sub>
I	Seek	0	0	0	1	h	V	r <sub>1</sub>	r <sub>0</sub>	0	0	0	1	h	V	r <sub>1</sub>	r <sub>0</sub>
I	Step	0	0	1	T	h	V	r <sub>1</sub>	r <sub>0</sub>	0	0	1	T	h	V	r <sub>1</sub>	r <sub>0</sub>
I	Step-in	0	1	0	T	h	V	r <sub>1</sub>	r <sub>0</sub>	0	1	0	T	h	V	r <sub>1</sub>	r <sub>0</sub>
I	Step-out	0	1	1	T	h	V	r <sub>1</sub>	r <sub>0</sub>	0	1	1	T	h	V	r <sub>1</sub>	r <sub>0</sub>
II	Read Sector	1	0	0	m	S	E	C	0	1	0	0	m	L	E	U	0
II	Write Sector	1	0	1	m	S	E	C	a <sub>0</sub>	1	0	1	m	L	E	U	a <sub>0</sub>
III	Read Address	1	1	0	0	0	E	0	0	1	1	0	0	0	E	U	0
III	Read Track	1	1	1	0	0	E	0	0	1	1	1	0	0	E	U	0
III	Write Track	1	1	1	1	0	E	0	0	1	1	1	1	0	E	U	0
IV	Force Interrupt	1	1	0	1	i <sub>3</sub>	i <sub>2</sub>	i <sub>1</sub>	i <sub>0</sub>	1	1	0	1	i <sub>3</sub>	i <sub>2</sub>	i <sub>1</sub>	i <sub>0</sub>

**FLAG SUMMARY**

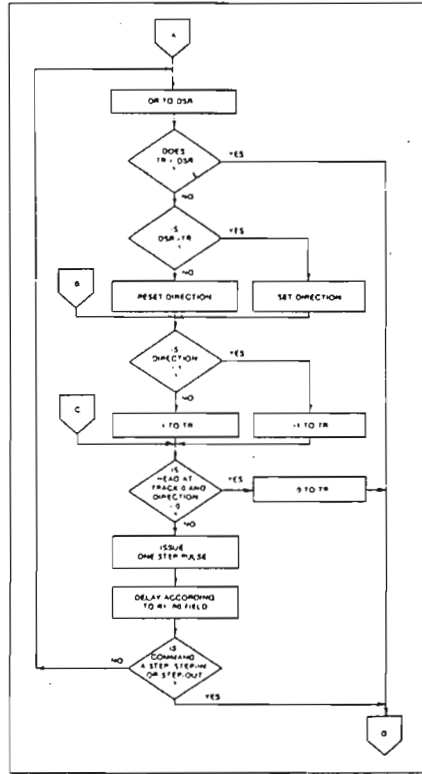
**TABLE 2. FLAG SUMMARY**

Command Type	Bit No(s)		Description																				
I	0, 1	r <sub>1</sub> r <sub>0</sub> = Stepping Motor Rate See Table 3 for Rate Summary																					
I	2	V = Track Number Verify Flag	V = 0, No verify V = 1, Verify on destination track																				
I	3	h = Head Load Flag	h = 1, Load head at beginning h = 0, Unload head at beginning																				
I	4	T = Track Update Flag	T = 0, No update T = 1, Update track register																				
II	0	a <sub>0</sub> = Data Address Mark	a <sub>0</sub> = 0, FB (DAM) a <sub>0</sub> = 1, FB (deleted DAM)																				
II	1	C = Side Compare Flag	C = 0, Disable side compare C = 1, Enable side compare																				
II & III	1	U = Update SSO	U = 0, Update SSO to 0 U = 1, Update SSO to 1																				
II & III	2	E = 15 MS Delay	E = 0, No 15 MS delay E = 1, 15 MS delay																				
II	3	S = Side Compare Flag	S = 0, Compare for side 0 S = 1, Compare for side 1																				
II	3	L = Sector Length Flag	<table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th colspan="5">LSB's Sector Length in ID Field</th> </tr> <tr> <th></th> <th>00</th> <th>01</th> <th>10</th> <th>11</th> </tr> </thead> <tbody> <tr> <td>L = 0</td> <td>256</td> <td>512</td> <td>1024</td> <td>128</td> </tr> <tr> <td>L = 1</td> <td>128</td> <td>256</td> <td>512</td> <td>1024</td> </tr> </tbody> </table>	LSB's Sector Length in ID Field						00	01	10	11	L = 0	256	512	1024	128	L = 1	128	256	512	1024
LSB's Sector Length in ID Field																							
	00	01	10	11																			
L = 0	256	512	1024	128																			
L = 1	128	256	512	1024																			
II	4	m = Multiple Record Flag	m = 0, Single record m = 1, Multiple records																				
IV	0-3	i <sub>x</sub> = Interrupt Condition Flags i <sub>0</sub> = 1 Not Ready To Ready Transition i <sub>1</sub> = 1 Ready To Not Ready Transition i <sub>2</sub> = 1 Index Pulse i <sub>3</sub> = 1 Immediate Interrupt, Requires A Reset i <sub>3</sub> i <sub>0</sub> = 0 Terminate With No Interrupt (INTRQ)																					

\*NOTE: See Type IV Command Description for further information.



TYPE I COMMAND FLOW



TYPE I COMMAND FLOW

TYPE I COMMANDS

The Type I Commands include the Restore, Seek, Step, Step-In, and Step-Out commands. Each of the Type I Commands contains a rate field (R1), which determines the stepping motor rate as defined in Table 3.

A 2 μs (MFM) or 4 μs (FM) pulse is provided as an output to the drive. For every step pulse issued, the drive moves one track location in a direction determined by the direction output. The chip will step the drive in the same direction it last stepped unless the command changes the direction.

The Direction signal is active high when stepping in and low when stepping out. The Direction signal is valid 12 μs before the first stepping pulse is generated.

The rates (shown in Table 3) can be applied to a Step-Direction Motor through the device interface.

TABLE 3. STEPPING RATES

CLK	2 MHz	2 MHz	1 MHz	1 MHz	2 MHz	1 MHz
DOEN	0	1	0	1	X	X
R1 R0	TEST+1	TEST+1	TEST+1	TEST+1	TEST-0	TEST-0
0 0	3 ms	3 ms	6 ms	6 ms	184 μs	368 μs
0 1	8 ms	6 ms	12 ms	12 ms	190 μs	380 μs
1 0	10 ms	10 ms	20 ms	20 ms	198 μs	396 μs
1 1	15 ms	15 ms	30 ms	30 ms	208 μs	416 μs

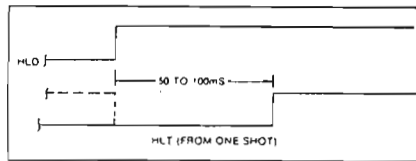
After the last directional step an additional 15 milliseconds of head settling time takes place if the Verify flag is set in Type I commands. Note that this time doubles to 30 ms for a 1 MHz clock. If TEST = 0, there is zero settling time. There is also a 15 ms head settling time if the E flag is set in any Type II or III command.

When a Seek, Step or Restore command is executed an optional verification of Read-Write head position can be performed by settling bit 2 (V = 1) in the command word to a logic 1. The verification operation begins at the end of the 15 millisecond settling time after the head is loaded against the media. The track number from the first encountered ID Field is compared against the contents of the Track Register. If the track numbers compare and the ID Field Cyclic Redundancy Check (CRC) is correct, the verify operation is complete and an INTRQ is generated with no errors. If there is a match but not a valid CRC, the CRC error status bit is set (Status bit 3), and the next encountered ID field is read from the disk for the verification operation.

The FD179X must find an ID field with correct track number and correct CRC within 5 revolutions of the media; otherwise the seek error is set and an INTRQ is generated. If V = 0, no verification is performed.

The Head Load (HLD) output controls the movement of the read/write head against the media. HLD is activated at the beginning of a Type I command if the h flag is set (h = 1), at the end of the Type I command if the verify flag (V = 1), or upon receipt of any Type II or III command. Once HLD is active it remains active until either a Type I command is received with (h = 0 and V = 0); or if the FD179X is in an idle state (non-busy) and 15 index pulses have occurred.

Head Load timing (HLT) is an input to the FD179X which is used for the head engage time. When HLT = 1, the FD179X assumes the head is completely engaged. The head engage time is typically 30 to 100 ms depending on drive. The low to high transition on HLT is typically used to fire a one shot. The output of the one shot is then used for HLT and supplied as an input to the FD179X.



HEAD LOAD TIMING

When both HLD and HLT are true, the FD179X will then read from or write to the media. The "and" of HLD and HLT appears as status Bit 5 in Type I status.

In summary for the Type I commands: if h = 0 and V = 0, HLD is reset. If h = 1 and V = 0, HLD is set at the beginning of the command and HLT is not sampled nor is there an internal 15 ms delay. If h = 0 and V = 1, HLD is set near the end of the command, an internal 15 ms occurs, and the FD179X waits for HLT to be true. If h = 1 and V = 1, HLD is set at the beginning of the command. Near the end of the command, after all the steps have been issued, an internal 15 ms delay occurs and the FD179X then waits for HLT to occur.

For Type II and III commands with E flag off, HLD is made active and HLT is sampled until true. With E flag on, HLD is made active, an internal 15 ms delay occurs and then HLT is sampled until true.

RESTORE (SEEK TRACK 0)

Upon receipt of this command the Track 00 (TR00) input is sampled. If TR00 is active low indicating the Read-Write head is positioned over track 0, the Track Register is loaded with zeroes and an interrupt is generated. If TR00 is not active low, stepping pulses (pins 15 to 16) at a rate specified by the r1 r0 field are issued until the TR00 input is activated. At this time the Track Register is loaded with zeroes and an interrupt is generated. If the TR00 input does not go active low after 255 stepping pulses, the FD179X terminates operation, interrupts, and sets the Seek error status bit, providing the V flag is set. A verification operation also takes place if the V flag is set. The h bit allows the head to be loaded at the start of command. Note that the Restore command is executed when MR goes from an active to an inactive state and that the DRQ pin stays low.

SEEK

This command assumes that the Track Register contains the track number of the current position of the Read-Write head and the Data Register contains the desired track number. The FD179X will update the Track register and issue stepping pulses in the appropriate direction until the contents of the Track register are equal to the contents of

the Data Register (the desired track location). A verification operation takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command. Note: When using multiple drives, the track register must be updated for the drive selected before seeks are issued.

STEP

Upon receipt of this command, the FD179X issues one stepping pulse to the disk drive. The stepping motor direction is the same as in the previous step command. After a delay determined by the f10 field, a verification takes place if the V flag is on. If the U flag is on, the Track Register is updated. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

STEP-IN

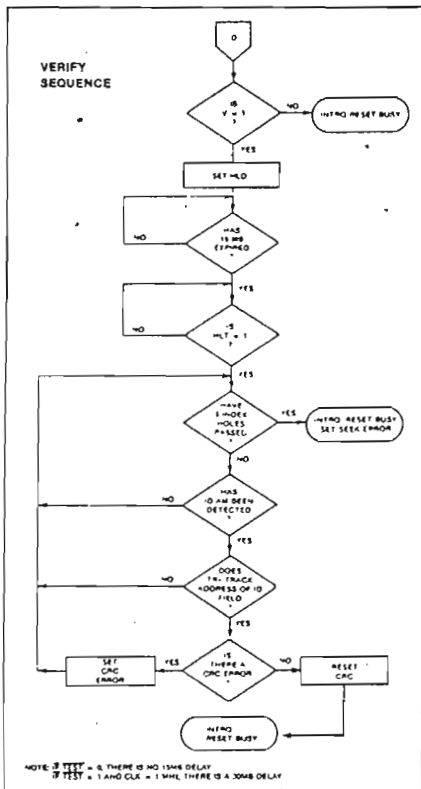
Upon receipt of this command, the FD179X issues one stepping pulse in the direction towards track 76. If the U flag is on, the Track Register is incremented by one. After a delay determined by the f10 field, a verification takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

STEP-OUT

Upon receipt of this command, the FD179X issues one stepping pulse in the direction towards track 0. If the U flag is on, the Track Register is decremented by one. After a delay determined by the f10 field, a verification takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

EXCEPTIONS

On the 1795/7 devices, the SSO output is not affected during Type 1 commands, and an internal side compare does not take place when the (V) Verify Flag is on.

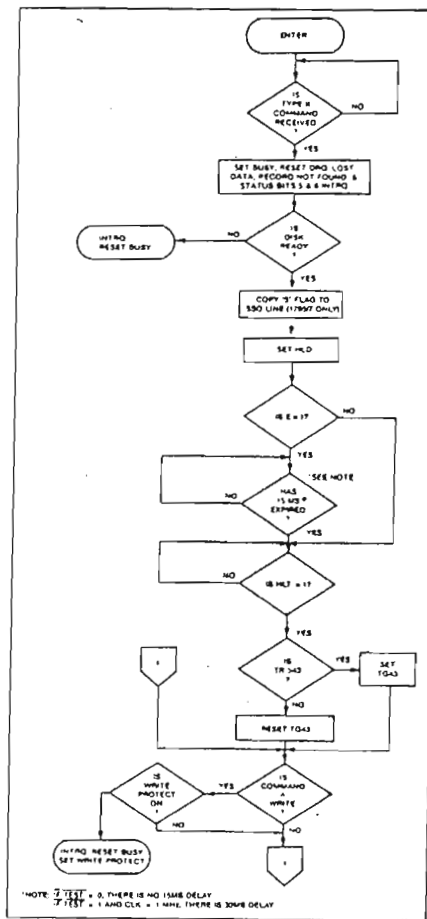


TYPE I COMMAND FLOW

TYPE II COMMANDS

The Type II Commands are the Read Sector and Write Sector commands. Prior to loading the Type II Command into the Command Register, the computer must load the Sector Register with the desired sector number. Upon receipt of the Type II command, the busy status Bit is set. If the E flag = 1 (this is the normal case) HLD is made active and HLT is sampled after a 15 msec delay. If the E flag is 0, the head is loaded and HLT sampled with no 15 msec delay. The ID field and Data Field format are shown on page 13.

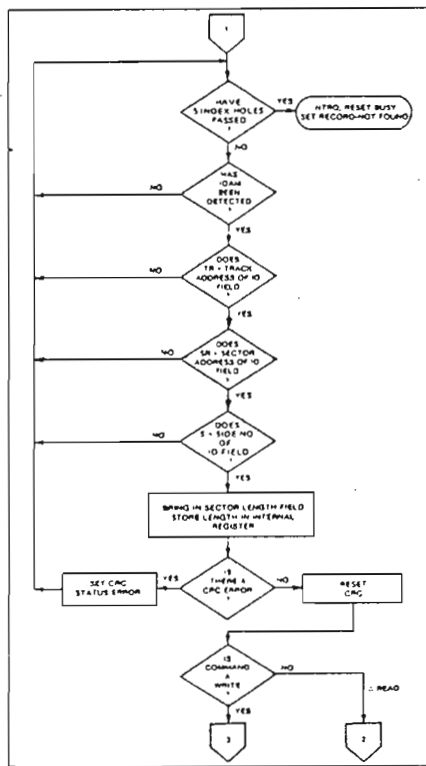
When an ID field is located on the disk, the FD179X compares the Track Number on the ID field with the Track Register. If there is not a match, the next encountered ID field is read and a comparison is again made. If there was a match, the Sector Number of the ID field is compared with the Sector Register. If there is not a Sector match, the next encountered ID field is read off the disk and comparisons again made. If the ID field CRC is correct, the data field is then located and will be either written into, or read from depending upon the command. The FD179X must find an ID field with a Track number, Sector number, side number, and CRC within four revolutions of the disk; otherwise, the Record not found status bit is set (Status bit 3) and the command is terminated with an interrupt.



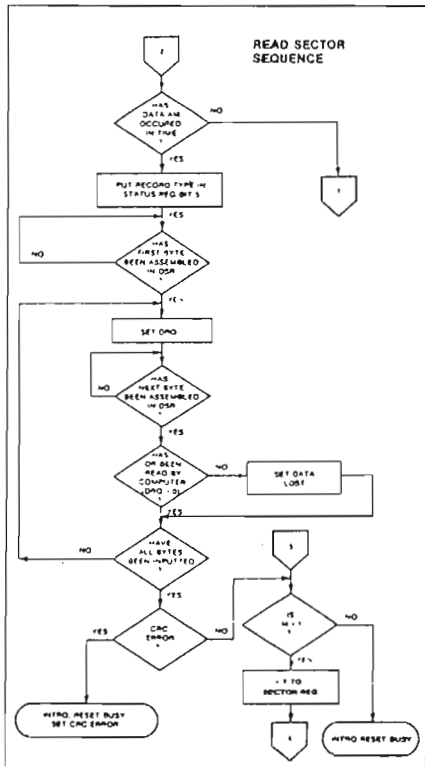
TYPE II COMMAND

Each of the Type II Commands contains an (m) flag which determines if multiple records (sectors) are to be read or written, depending upon the command. If m = 0, a single sector is read or written and an interrupt is generated at the completion of the command. If m = 1, multiple records are read or written with the sector register internally updated so that an address verification can occur on the next record. The FD179X will continue to read or write multiple records and update the sector register in numerical ascending sequence until the sector register exceeds the number of sectors on the track or until the Force Interrupt command is loaded into the Command Register, which terminates the command and generates an interrupt.

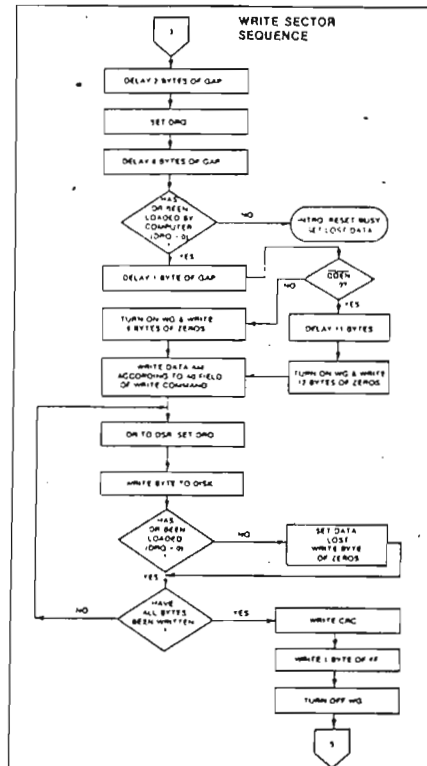
For example: If the FD179X is instructed to read sector 27 and there are only 26 on the track, the sector register exceeds the number available. The FD179X will search for 5 disk revolutions, interrupt out, reset busy, and set the record not found status bit.



TYPE II COMMAND



TYPE II COMMAND



TYPE II COMMAND

The Type II commands for 1791-94 also contain side select compare flags. When C = 0 (Bit 1) no side comparison is made. When C = 1, the LSB of the side number is read off the ID Field of the disk and compared with the contents of the (S) flag (Bit 3). If the S flag compares with the side number recorded in the ID field, the FD179X continues with the ID search. If a comparison is not made within 5 index pulses, the interrupt line is made active and the Record-Not-Found status bit is set.

The Type II and III commands for the 1795-97 contain a side select flag (Bit 1). When U = 0, SSO is updated to 0. Similarly, U = 1 updates SSO to 1. The chip compares the SSO to the ID field. If they do not compare within 5 revolutions the interrupt line is made active and the RNF status bit is set.

The 1795/7 READ SECTOR and WRITE SECTOR commands include a 'L' flag. The 'L' flag, in conjunction with the sector length byte of the ID Field, allows different byte lengths to be implemented in each sector. For IBM compatibility, the 'L' flag should be set to a one.

**READ SECTOR**

Upon receipt of the Read Sector command, the head is loaded, the Busy status bit set, and when an ID field is encountered that has the correct track number, correct sector number, correct side number, and correct CRC, the data field is presented to the computer. The Data Address

Mark of the data field must be found within 30 bytes in single density and 43 bytes in double density of the last ID field CRC byte; if not, the ID field is searched for and verified again followed by the Data Address Mark search. If after 5 revolutions the DAM cannot be found, the Record Not Found status bit is set and the operation is terminated. When the first character or byte of the data field has been shifted through the DSR, it is transferred to the DR, and DRQ is generated. When the next byte is accumulated in the DSR, it is transferred to the DR and another DRQ is generated. If the Computer has not read the previous contents of the DR before a new character is transferred that character is lost and the Lost Data Status bit is set. This sequence continues until the complete data field has been inputted to the computer. If there is a CRC error at the end of the data field, the CRC error status bit is set, and the command is terminated (even if it is a multiple record command).

At the end of the Read operation, the type of Data Address Mark encountered in the data field is recorded in the Status Register (Bit 5) as shown:

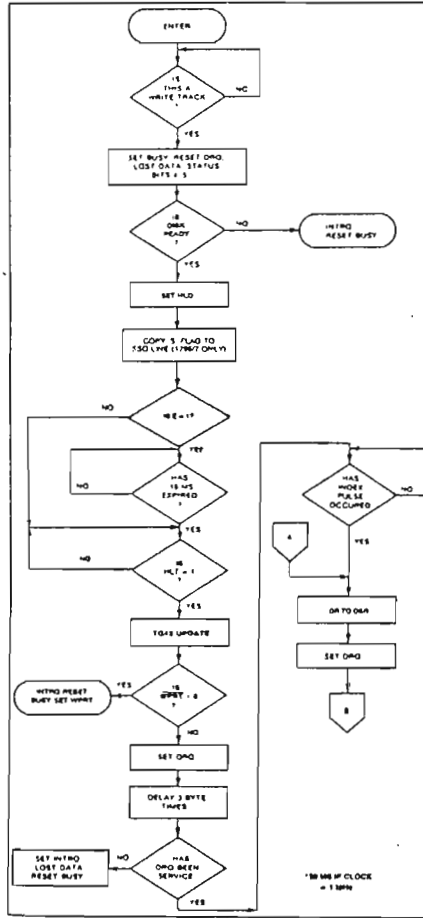
STATUS BIT 5	
1	Deleted Data Mark
0	Data Mark

**WRITE SECTOR**

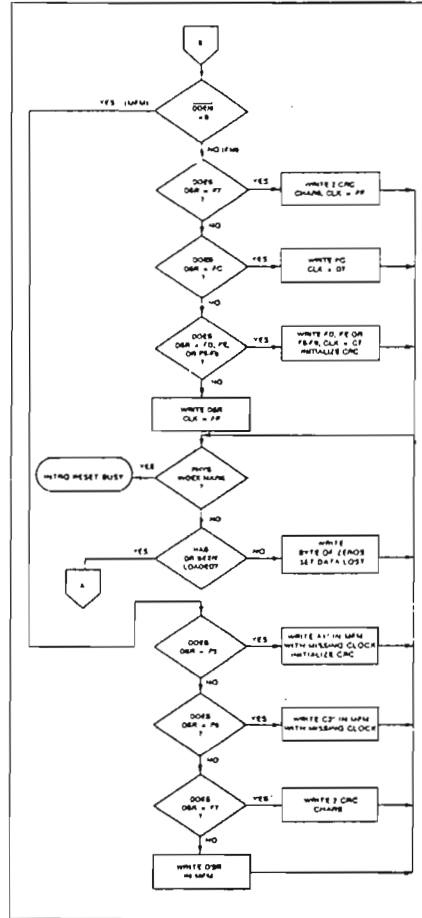
Upon receipt of the Write Sector command, the head is loaded (HLD active) and the Busy status bit is set. When an ID field is encountered that has the correct track number, correct sector number, correct side number, and correct CRC, a DRQ is generated. The FD179X counts off 11 bytes in single density and 22 bytes in double density from the CRC field and the Write Gate (WG) output is made active if the DRQ is serviced (i.e., the DR has been loaded by the computer). If DRQ has not been serviced, the command is terminated and the Lost Data status bit is set. If the DRQ has been serviced, the WG is made active and six bytes of zeroes in single density and 12 bytes in double density are then written on the disk. At this time the Data Address Mark is then written on the disk as determined by the  $\alpha_0$  field of the command as shown below:

$\alpha_0$ Data Address Mark (Bit 0)	
1	Deleted Data Mark
0	Data Mark

The FD179X then writes the data field and generates DRQ's to the computer. If the DRQ is not serviced in time for continuous writing the Lost Data Status Bit is set and a byte of zeroes is written on the disk. The command is not terminated. After the last data byte has been written on the disk, the two-byte CRC is computed internally and written on the disk followed by one byte of logic ones in FM or in MFM. The WG output is then deactivated. For a 2 MHz clock the INTRQ will set 8 to 12  $\mu$ sec after the last CRC byte is written. For partial sector writing, the proper method is to write the data and fill the balance with zeroes. By letting the chip fill the zeroes, errors may be masked by the lost data status and improper CRC Bytes.



TYPE III COMMAND WRITE TRACK



TYPE III COMMAND WRITE TRACK

TYPE III COMMANDS

READ ADDRESS

Upon receipt of the Read Address command, the head is loaded and the Busy Status Bit is set. The next encountered ID field is then read in from the disk, and the six data bytes of the ID field are assembled and transferred to the DR, and a DRO is generated for each byte. The six bytes of the ID field are shown below:

TRACK ADDR	SIDE NUMBER	SECTOR ADDRESS	SECTOR LENGTH	CRC 1	CRC 2
1	2	3	4	5	6

Although the CRC characters are transferred to the computer, the FD179X checks for validity and the CRC error status bit is set if there is a CRC error. The Track Address of the ID field is written into the sector register so that a comparison can be made by the user. At the end of the operation an interrupt is generated and the Busy Status is reset.

READ TRACK

Upon receipt of the READ track command, the head is loaded, and the Busy Status bit is set. Reading starts with the leading edge of the first encountered Index pulse and continues until the next index pulse. All Gap, Header, and data bytes are assembled and transferred to the data register and DRO's are generated for each byte. The accumulation of bytes is synchronized to each address mark encountered. An interrupt is generated at the completion of the command.

This command has several characteristics which make it suitable for diagnostic purposes. They are: the Read Gate

is not activated during the command; no CRC checking is performed; gap information is included in the data stream; the internal side compare is not performed; and the address mark detector is on for the duration of the command. Because the A.M. detector is always on, write splices or noise may cause the chip to look for an A.M. If an address mark does not appear on schedule the Lost Data status flag is set.

The ID A.M., ID field, ID CRC bytes, DAM, Data, and Data CRC Bytes for each sector will be correct. The Gap Bytes may be read incorrectly during write-splice time because of synchronization.

CONTROL BYTES FOR INITIALIZATION

DATA PATTERN IN DR (HEX)	FD179X INTERPRETATION IN FM (ODEN = 1)	FD1791/3 INTERPRETATION IN MFM (ODEN = 0)
00 thru F4	Write 00 thru F4 with CLK = FF	Write 00 thru F4, in MFM
F5	Not Allowed	Write A1* in MFM, Preset CRC
F6	Not Allowed	Write C2** in MFM
F7	Generate 2 CRC bytes	Generate 2 CRC bytes
F8 thru FB	Write F8 thru FB, Clk = C7, Preset CRC	Write F8 thru FB, in MFM
FC	Write FC with Clk = D7	Write FC in MFM
FD	Write FD with Clk = FF	Write FD in MFM
FE	Write FE, Clk = C7, Preset CRC	Write FE in MFM
FF	Write FF with Clk = FF	Write FF in MFM

\*Missing clock transition between bits 4 and 5

\*\*Missing clock transition between bits 3 & 4

**WRITE TRACK FORMATTING THE DISK**

(Refer to section on Type III commands for flow diagrams.)

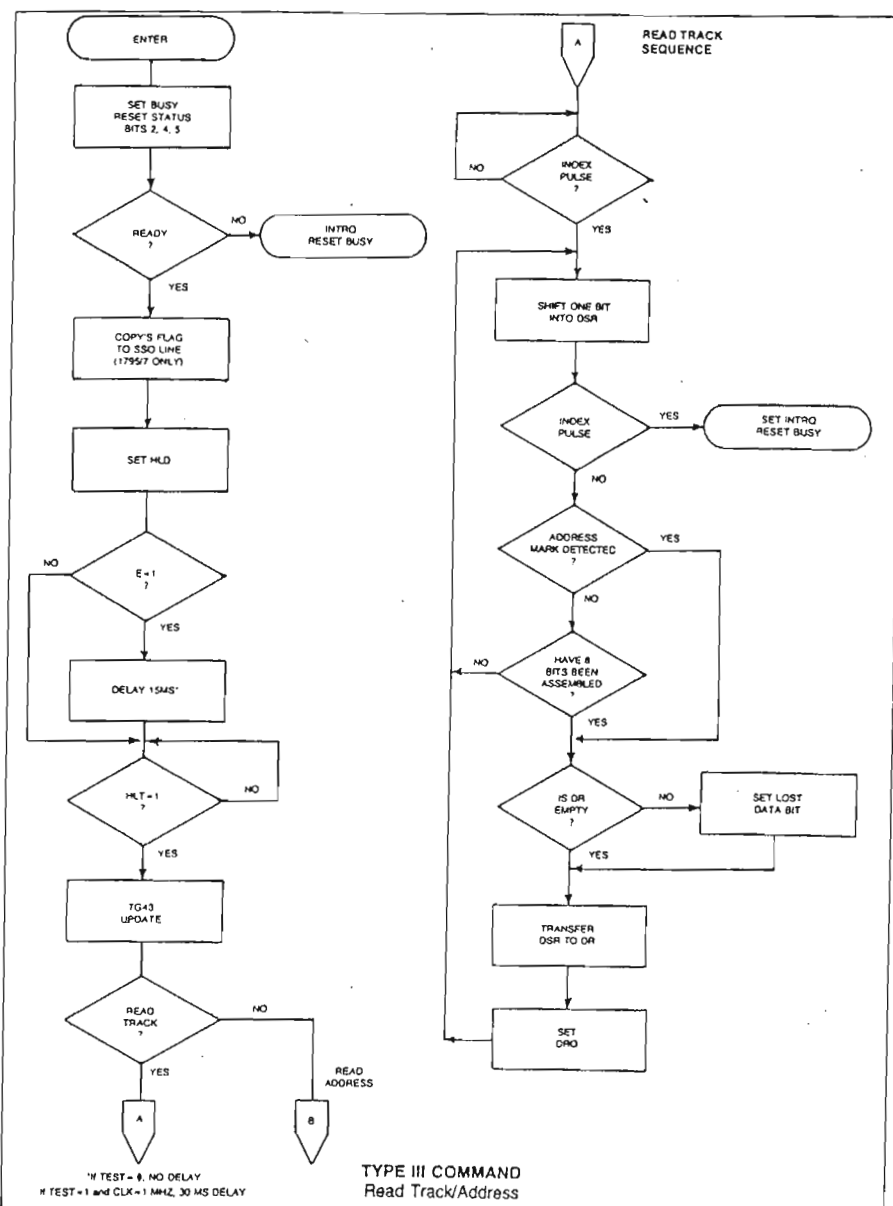
Formatting the disk is a relatively simple task when operating programmed I/O or when operating under DMA with a large amount of memory. Data and gap information must be provided at the computer interface. Formatting the disk is accomplished by positioning the R/W head over the desired track number and issuing the Write Track command.

Upon receipt of the Write Track command, the head is loaded and the Busy Status bit is set. Writing starts with the leading edge of the first encountered index pulse and continues until the next index pulse, at which time the Interrupt is activated. The Data Request is activated immediately upon receiving the command, but writing will not start until after the first byte has been loaded into the Data Register. If the DR has not been loaded by the time the index pulse is encountered the operation is terminated making the device Not Busy, the Lost Data Status Bit is set, and the Interrupt is activated. If a byte is not present in the DR when needed, a byte of zeroes is substituted.

This sequence continues from one index mark to the next index mark. Normally, whatever data pattern appears in the data register is written on the disk with a normal clock pattern. However, if the FD179X detects a data pattern of F5 thru FE in the data register, this is interpreted as data address marks with missing clocks or CRC generation.

The CRC generator is initialized when any data byte from F8 to FE is about to be transferred from the DR to the DSR in FM or by receipt of F5 in MFM. An F7 pattern will generate two CRC characters in FM or MFM. As a consequence, the patterns F5 thru FE must not appear in the gaps, data fields, or ID fields. Also, CRC's must be generated by an F7 pattern.

Disks may be formatted in IBM 3740 or System 34 formats with sector lengths of 128, 256, 512, or 1024 bytes.



**TYPE IV COMMANDS**

The Forced Interrupt command is generally used to terminate a multiple sector read or write command or to insure Type I status in the status register. This command can be loaded into the command register at any time. If there is a current command under execution (busy status bit set), the command will be terminated and the busy status bit reset.

The lower four bits of the command determine the conditional interrupt as follows:

- I<sub>0</sub> = Not-Ready to Ready Transition
- I<sub>1</sub> = Ready to Not-Ready Transition
- I<sub>2</sub> = Every Index Pulse
- I<sub>3</sub> = Immediate Interrupt

The conditional interrupt is enabled when the corresponding bit positions of the command (I<sub>3</sub> - I<sub>0</sub>) are set to a 1. Then, when the condition for interrupt is met, the INTRQ line will go high signifying that the condition specified has occurred. If I<sub>3</sub> - I<sub>0</sub> are all set to zero (HEX D0), no interrupt will occur but any command presently under execution will be immediately terminated. When using the immediate interrupt condition (I<sub>3</sub> = 1) an interrupt will be immediately generated and the current command terminated. Reading the status or writing to the command register will not automatically clear the interrupt. The HEX D0 is the only command that will enable the immediate interrupt (HEX D8) to clear on a subsequent load command register or read status register operation. Follow a HEX D8 with D0 command.

Wait 8 micro sec (double density) or 16 micro sec (single density) before issuing a new command after issuing a forced interrupt (times double when clock = 1 MHz). Loading a new command sooner than this will nullify the forced interrupt.

Forced interrupt stops any command at the end of an internal micro-instruction and generates INTRQ when the specified condition is met. Forced interrupt will wait until ALU operations in progress are complete (CRC calculations, compares, etc.).

More than one condition may be set at a time. If for example, the READY TO NOT-READY condition (I<sub>1</sub> = 1) and the Every Index Pulse (I<sub>2</sub> = 1) are both set, the resultant command would be HEX "DA". The "OR" function is performed so that either a READY TO NOT-READY or the next Index Pulse will cause an interrupt condition.

**STATUS REGISTER**

Upon receipt of any command, except the Force Interrupt command, the Busy Status bit is set and the rest of the status bits are updated or cleared for the new command. If the Force Interrupt Command is received when there is a current command under execution, the Busy status bit is reset, and the rest of the status bits are unchanged. If the Force Interrupt command is received when there is not a current command under execution, the Busy Status bit is reset and the rest of the status bits are updated or cleared. In this case, Status reflects the Type I commands.

The user has the option of reading the status register through program control or using the DRQ line with DMA or interrupt methods. When the Data register is read the DRQ bit in the status register and the DRQ line are automatically reset. A write to the Data register also causes both DRQ's to reset.

The busy bit in the status may be monitored with a user program to determine when a command is complete. In lieu of using the INTRQ line. When using the INTRQ, a busy status check is not recommended because a read of the status register to determine the condition of busy will reset the INTRQ line.

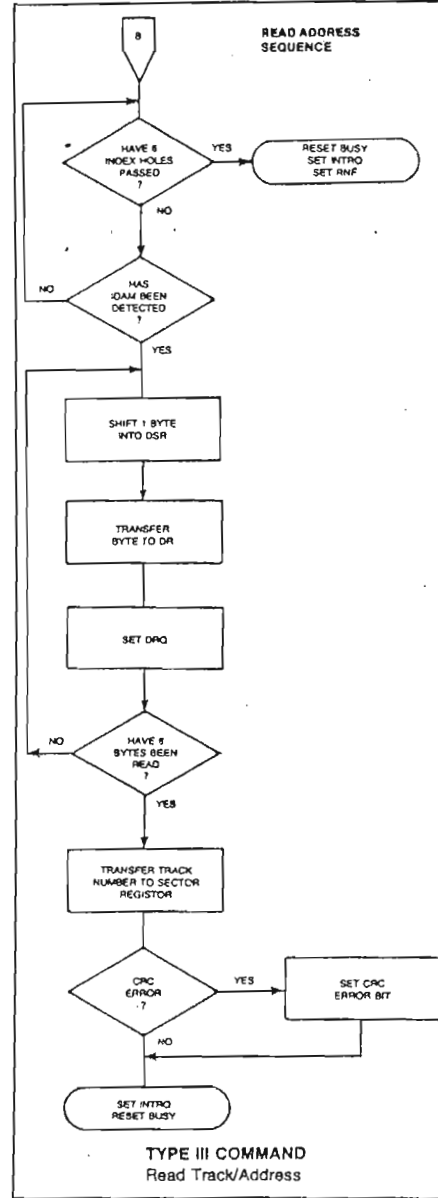
The format of the Status Register is shown below:

(BITS)							
7	6	5	4	3	2	1	0
S7	S6	S5	S4	S3	S2	S1	S0

Status varies according to the type of command executed as shown in Table 4.

Because of internal sync cycles, certain time delays must be observed when operating under programmed I/O. They are: (times double when clock = 1 MHz)

Operation	Next Operation	Delay Req'd.	
		FM	MFM
Write to Command Reg.	Read Busy Bit (Status Bit 0)	12 μs	6 μs
Write to Command Reg.	Read Status Bits 1-7	28 μs	14 μs
Write Any Register	Read From Diff. Register	0	0



**IBM 3740 FORMAT — 128 BYTES/SECTOR**

Shown below is the IBM single-density format with 128 bytes/sector. In order to format a diskette, the user must issue the Write Track command, and load the data register with the following values. For every byte to be written, there is one Data Request.

**IBM 3740 FORMAT — 128 BYTES/SECTOR**

Shown below is the IBM single-density format with 128 bytes/sector. In order to format a diskette, the user must issue the Write Track command, and load the data register with the following values. For every byte to be written, there is one Data Request.

NUMBER OF BYTES	HEX VALUE OF BYTE WRITTEN
40	FF (or 00)*
6	00
1	FC (Index Mark)
26	FF (or 00)*
6	00
1	FE (ID Address Mark)
1	Track Number
1	Side Number (00 or 01)
1	Sector Number (1 thru 1A)
1	00 (Sector Length)
1	F7 (2 CRC's written)
11	FF (or 00)*
6	00
1	FB (Data Address Mark)
128	Data (IBM uses E5)
1	F7 (2 CRC's written)
27	FF (or 00)*
247**	FF (or 00)*

\*Write bracketed field 26 times

\*\*Continue writing until FD179X interrupts out. Approx. 247 bytes.

1-Optional '00' on 1795/7 only.

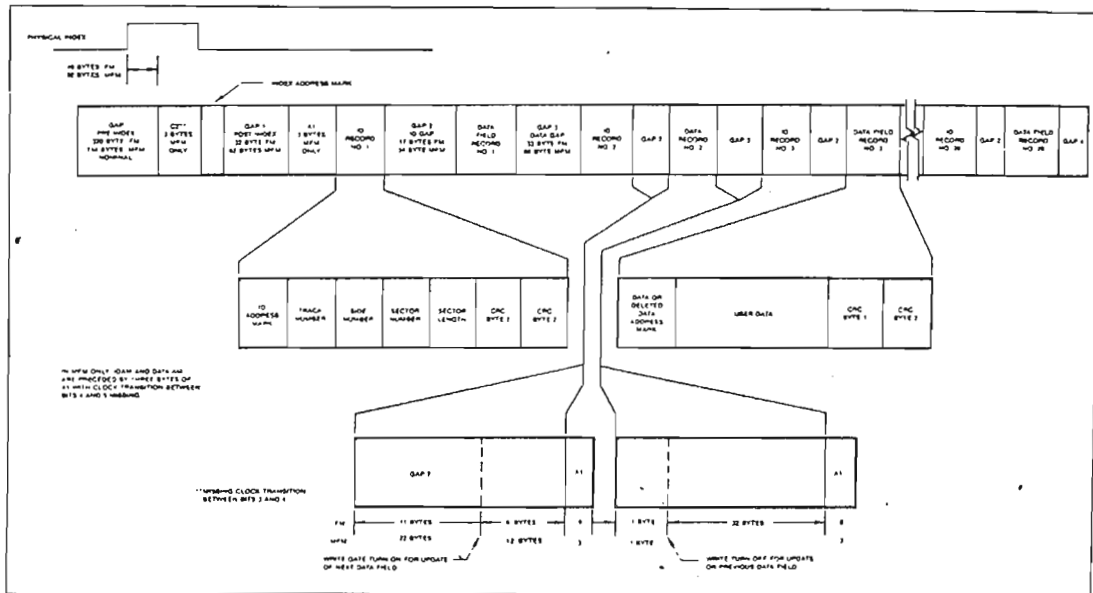


**IBM SYSTEM 34 FORMAT- 256 BYTES/SECTOR**

Shown below is the IBM dual-density format with 256 bytes/sector. In order to format a diskette the user must issue the Write Track command and load the data register with the following values. For every byte to be written, there is one data request.

NUMBER OF BYTES	HEX VALUE OF BYTE WRITTEN
80	4E
12	00
3	F6 (Writes C2)
1	FC (Index Mark)
* 50	4E
12	00
3	F5 (Writes A1)
1	FE (ID Address Mark)
1	Track Number (0 thru 4C)
1	Side Number (0 or 1)
1	Sector Number (1 thru 1A)
1	01 (Sector Length)
1	F7 (2 CRCs written)
22	4E
12	00
3	F5 (Writes A1)
1	FB (Data Address Mark)
256	DATA
1	F7 (2 CRCs written)
54	4E
598**	4E

\*Write bracketed field 26 times  
 \*\*Continue writing until FD179X interrupts out. Approx. 598 bytes.



**IBM TRACK FORMAT**

**1. NON-IBM FORMATS**

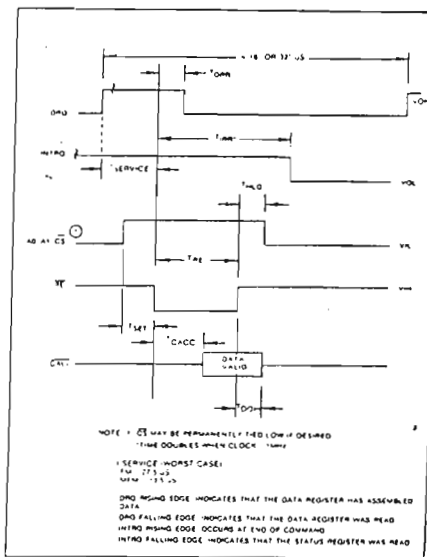
Variations in the IBM formats are possible to a limited extent if the following requirements are met:

- 1) Sector size must be 128, 256, 512 or 1024 bytes.
- 2) Gap 2 cannot be varied from the IBM format.
- 3) 3 bytes of A1 must be used in MFM.

In addition, the Index Address Mark is not required for operation by the FD179X. Gap 1, 3, and 4 lengths can be as short as 2 bytes for FD179X operation, however PLL lock up time, motor speed variation, write-splice area, etc. will add more bytes to each gap to achieve proper operation. It is recommended that the IBM format be used for highest system reliability.

	FM	MFM
Gap I	16 bytes FF	32 bytes 4E
Gap II	11 bytes FF	22 bytes 4E
.	6 bytes 00	12 bytes 00
.		3 bytes A1
Gap III**	10 bytes FF 4 bytes 00	24 bytes 4E 8 bytes 00
Gap IV	16 bytes FF	16 bytes 4E

\*Byte counts must be exact.  
 \*\*Byte counts are minimum, except exactly 3 bytes of A1 must be written.



**READ ENABLE TIMING**

**TIMING CHARACTERISTICS**

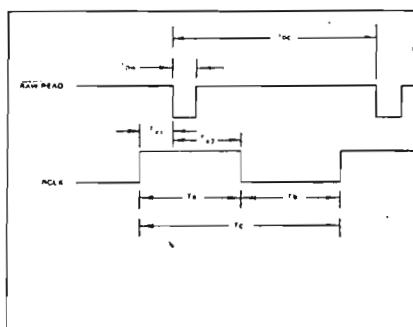
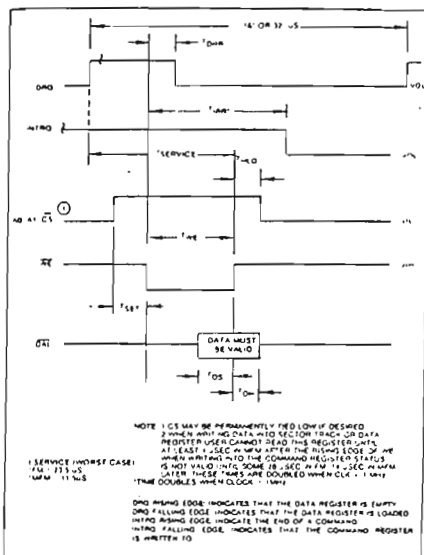
T<sub>A</sub> = 0°C to 70°C, V<sub>DD</sub> = +12V ± .6V, V<sub>SS</sub> = 0V, V<sub>CC</sub> = +5V ± .25V

**READ ENABLE TIMING** (See Note 6, Page 21)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
TSET	Setup ADDR & CS to $\overline{RE}$	50			nsec	
THLD	Hold ADDR & CS from $\overline{RE}$	10			nsec	
TRE	$\overline{RE}$ Pulse Width	400			nsec	C <sub>L</sub> = 50 pf
TDRR	DRQ Reset from $\overline{RE}$		400	500	nsec	
TIRR	INTRQ Reset from $\overline{RE}$		500	3000	nsec	See Note 5
TDACC	Data Access from $\overline{RE}$			350	nsec	C <sub>L</sub> = 50 pf
TDOH	Data Hold From $\overline{RE}$	50		150	nsec	C <sub>L</sub> = 50 pf

**WRITE ENABLE TIMING** (See Note 6, Page 21)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
TSET	Setup ADDR & CS to $\overline{WE}$	50			nsec	
THLD	Hold ADDR & CS from $\overline{WE}$	10			nsec	
TWE	$\overline{WE}$ Pulse Width	350			nsec	
TDRR	DRQ Reset from $\overline{WE}$		400	500	nsec	
TIRR	INTRQ Reset from $\overline{WE}$		500	3000	nsec	See Note 5
TDS	Data Setup to $\overline{WE}$	250			nsec	
TDH	Data Hold from $\overline{WE}$	70			nsec	



DISKETTE	MODE	ODEN	CLK	NOMINAL		
				T <sub>d</sub>	T <sub>c</sub>	T <sub>d2</sub>
8"	MFM	0	2 MHz	1 μs	1 μs	2 μs
8"	FM	1	2 MHz	2 μs	2 μs	4 μs
5"	MFM	0	1 MHz	2 μs	2 μs	4 μs
5"	FM	1	1 MHz	4 μs	4 μs	8 μs

INPUT DATA TIMING

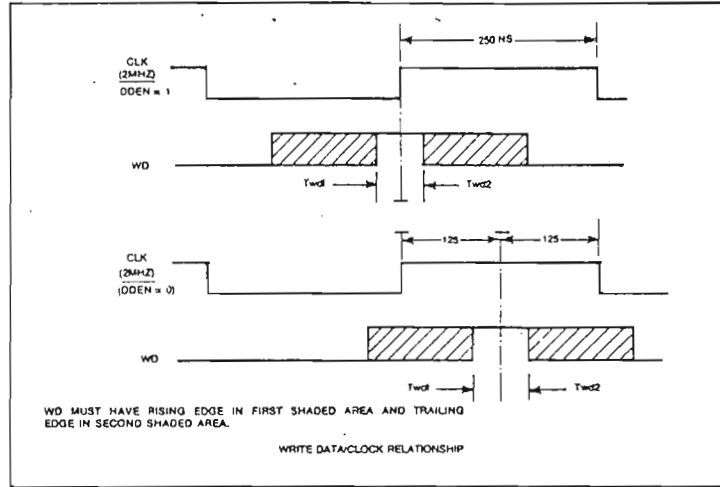
**WRITE ENABLE TIMING**

**INPUT DATA TIMING:**

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
Tpw	Raw Read Pulse Width	100	200		nsec	See Note 1
tbc	Raw Read Cycle Time	1500	2000		nsec	1800 ns @ 70°C
Tc	RCLK Cycle Time	1500	2000		nsec	1800 ns @ 70°C
Tx1	RCLK hold to Raw Read	40			nsec	See Note 1
Tx2	Raw Read hold to RCLK	40			nsec	See Note 1

**WRITE DATA TIMING: (ALL TIMES DOUBLE WHEN CLK = 1 MHz)** (See Note 6, Page 21)

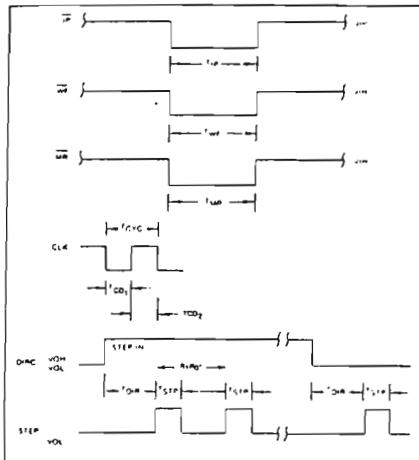
SYMBOL	CHARACTERISTICS	MIN.	TYP.	MAX.	UNITS	CONDITIONS
Twp	Write Data Pulse Width		500	650	nsec	FM
			200	350	nsec	MFM
Twg	Write Gate to Write Data		2		μsec	FM
			1		μsec	MFM
Tbc	Write data cycle Time		2,3, or 4		μsec	±CLK Error
Ts	Early (Late) to Write Data	125			nsec	MFM
Th	Early (Late) From Write Data	125			nsec	MFM
Twf	Write Gate off from WD		2		μsec	FM
			1		μsec	MFM
Twd1	WD Valid to Clk	100			nsec	CLK = 1 MHZ
		50			nsec	CLK = 2 MHZ
Twd2	WD Valid after CLK	100			nsec	CLK = 1 MHZ
		30			nsec	CLK = 2 MHZ



WRITE DATA TIMING

MISCELLANEOUS TIMING: (Times Double When Clock = 1 MHz) (See Note 6, Page 21)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
TCD <sub>1</sub>	Clock Duty (low)	230	250	20000	nsec	See Note 5 ± CLK ERROR
TCD <sub>2</sub>	Clock Duty (high)	200	250	20000	nsec	
TSTP	Step Pulse Output	2 or 4			μsec	
TDIR	Dir Setup to Step		12		μsec	
TMR	Master Reset Pulse Width	50			μsec	See Note 5
TIP	Index Pulse Width	10			μsec	
TWF	Write Fault Pulse Width	10			μsec	



MISCELLANEOUS TIMING

\*FROM STEP RATE TABLE

NOTES:

1. Pulse width on RAW READ (Pin 27) is normally 100-300 ns. However, pulse may be any width if pulse is entirely within window. If pulse occurs in both windows, then pulse width must be less than 300 ns for MFM at CLK = 2 MHz and 600 ns for FM at 2 MHz. Times double for 1 MHz.
2. A PPL Data Separator is recommended for 8" MFM.
3. tbc should be 2 μs, nominal in MFM and 4 μs nominal in FM. Times double when CLK = 1 MHz.
4. RCLK may be high or low during RAW READ (Polarity is unimportant).
5. Times double when clock = 1 MHz.
6. Output timing readings are at V<sub>OL</sub> = 0.8v and V<sub>OH</sub> = 2.0v.

Table 4. STATUS REGISTER SUMMARY

BIT	ALL TYPE I COMMANDS	READ ADDRESS	READ SECTOR	READ TRACK	WRITE SECTOR	WRITE TRACK
S7	NOT READY	NOT READY	NOT READY	NOT READY	NOT READY	NOT READY
S6	WRITE PROTECT	0	0	0	WRITE PROTECT	WRITE PROTECT
S5	HEAD LOADED	0	RECORD TYPE	0	WRITE FAULT	WRITE FAULT
S4	SEEK ERROR	RNF	RNF	0	RNF	0
S3	CRC ERROR	CRC ERROR	CRC ERROR	0	CRC ERROR	0
S2	TRACK 0	LOST DATA	LOST DATA	LOST DATA	LOST DATA	LOST DATA
S1	INDEX PULSE	DRQ	DRQ	DRQ	DRQ	DRQ
S0	BUSY	BUSY	BUSY	BUSY	BUSY	BUSY

STATUS FOR TYPE I COMMANDS

BIT NAME	MEANING
S7 NOT READY	This bit when set indicates the drive is not ready. When reset it indicates that the drive is ready. This bit is an inverted copy of the Ready input and logically 'ored' with MR.
S6 PROTECTED	When set, indicates Write Protect is activated. This bit is an inverted copy of WRPT input.
S5 HEAD LOADED	When set, it indicates the head is loaded and engaged. This bit is a logical "and" of HLD and HLT signals.
S4 SEEK ERROR	When set, the desired track was not verified. This bit is reset to 0 when updated.
S3 CRC ERROR	CRC encountered in ID field.
S2 TRACK 00	When set, indicates Read/Write head is positioned to Track 0. This bit is an inverted copy of the TROO input.
S1 INDEX	When set, indicates index mark detected from drive. This bit is an inverted copy of the IP input.
S0 BUSY	When set command is in progress. When reset no command is in progress.

## STATUS FOR TYPE II AND III COMMANDS

BIT NAME	MEANING
S7 NOT READY	This bit when set indicates the drive is not ready. When reset, it indicates that the drive is ready. This bit is an inverted copy of the Ready input and 'ored' with MR. The Type II and III Commands will not execute unless the drive is ready.
S6 WRITE PROTECT	On Read Record: Not Used. On Read Track: Not Used. On any Write: It indicates a Write Protect. This bit is reset when updated.
S5 RECORD TYPE/ WRITE FAULT	On Read Record: It indicates the record-type code from data field address mark. 1 = Deleted Data Mark. 0 = Data Mark. On any Write: It indicates a Write Fault. This bit is reset when updated.
S4 RECORD NOT FOUND (RNF)	When set, it indicates that the desired track, sector, or side were not found. This bit is reset when updated.
S3 CRC ERRCR	If S4 is set, an error is found in one or more ID fields; otherwise it indicates error in data field. This bit is reset when updated.
S2 LOST DATA	When set, it indicates the computer did not respond to DRQ in one byte time. This bit is reset to zero when updated.
S1 DATA REQUEST	This bit is a copy of the DRQ output. When set, it indicates the DR is full on a Read Operation or the DR is empty on a Write operation. This bit is reset to zero when updated.
S0 BUSY	When set, command is under execution. When reset, no command is under execution.

## ELECTRICAL CHARACTERISTICS

## Absolute Maximum Ratings

$V_{DD}$  with respect to  $V_{SS}$  (ground): +15 to -0.3V  
Voltage to any input with respect to  $V_{SS}$  = +15 to -0.3V  
 $I_{CC}$  = 60 mA (35 mA nominal)  
 $I_{OO}$  = 15 mA (10 mA nominal)

$C_{IN}$  &  $C_{OUT}$  = 15 pF max with all pins grounded except one under test.  
Operating temperature = 0°C to 70°C  
Storage temperature = -55°C to +125°C

## OPERATING CHARACTERISTICS (DC)

$T_A$  = 0°C to 70°C,  $V_{DD}$  = +12V  $\pm$  .6V,  $V_{SS}$  = 0V,  $V_{CC}$  = +5V  $\pm$  .25V

SYMBOL	CHARACTERISTIC	MIN.	MAX.	UNITS	CONDITIONS
$I_{IL}$	Input Leakage		10	$\mu$ A	$V_{IN} = V_{DD}^{**}$
$I_{OL}$	Output Leakage		10	$\mu$ A	$V_{OUT} = V_{DD}$
$V_{IH}$	Input High Voltage	2.6		V	
$V_{IL}$	Input Low Voltage		0.8	V	
$V_{OH}$	Output High Voltage	2.8		V	$I_O = -100 \mu$ A
$V_{OL}$	Output Low Voltage		0.45	V	$I_O = 1.6 \text{ mA}^*$
$P_D$	Power Dissipation		0.6	W	

\*1792 and 1794  $I_O = 1.0 \text{ mA}$

\*\*Leakage conditions are for input pins without internal pull-up resistors. Pins 22, 23, 33, 36, and 37 have pull-up resistors. See Tech Memo #115 for testing procedures.

2

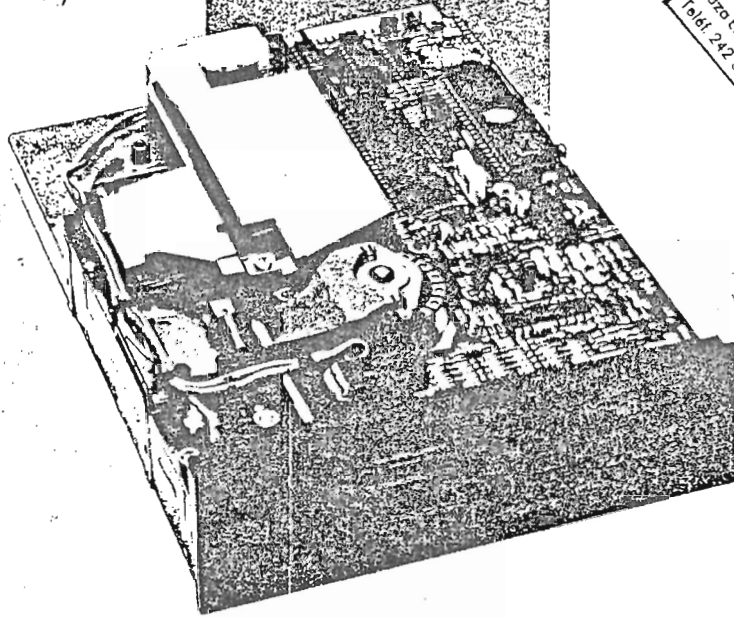
# Tandon

## TM65 SERIES THINLINE™

### FLEXIBLE DISK DRIVES

#### PRODUCT SPECIFICATION AND USER'S MANUAL

UNITRONICS S. A.  
Plaza España, 18, P.I. 12. O.I. 9  
Tel. 242 5204-MADRID-13



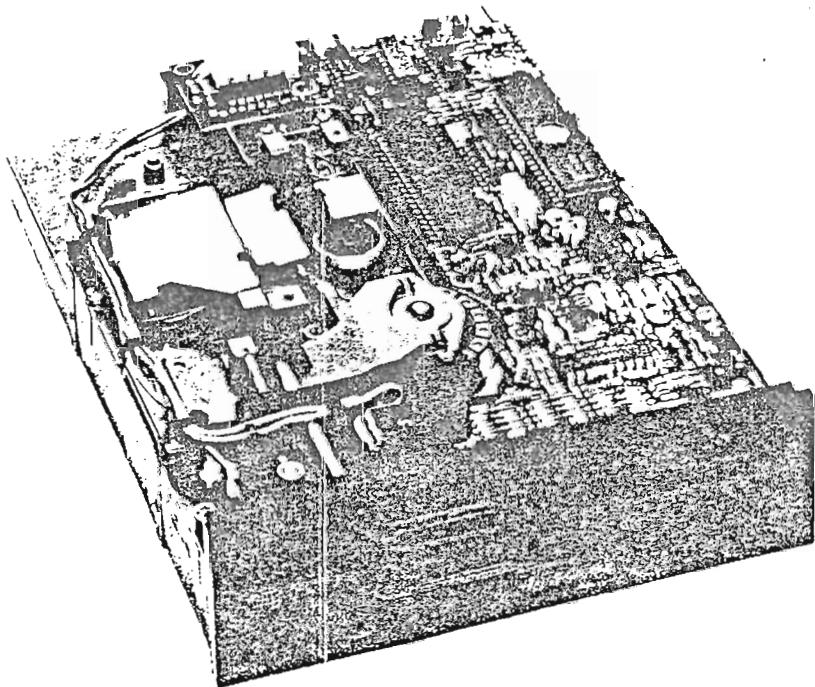
TM65 SERIES THINLINE™

5-1/4-INCH, SINGLE AND DOUBLE-SIDED, FLEXIBLE DISK DRIVES

48 AND 96 TRACKS PER INCH

PRODUCT SPECIFICATION AND USER'S MANUAL

TM65-4



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20320 PRAIRIE STREET  
CHATSWORTH, CALIFORNIA 91311

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# SECTION 1

## GENERAL DESCRIPTION

### INTRODUCTION

This manual provides useful information in order to evaluate and incorporate Tandon's disk drive into a system.

Tandon Corporation's TM65 series of drives are full feature, one-half height, 5-1/4-inch ThinLine™ flexible disk drives. The drives are compact data storage devices that use an ANSI-compatible, Industry Standard 5-1/4-inch diskette.

Model Number TM65-1L is a single-sided, 48 tracks per inch, recording device. The TM65-2L is a double-sided, 48 tracks per inch, recording device. Model Number TM65-4 is a double-sided, 96 tracks per inch, recording device.

The drives are capable of reading and writing digital data using FM, MFM, or MMFM techniques. Encoding and decoding of the data is done by the user's controller.

#### 1.1 SCOPE OF THE DOCUMENT

This document contains a description of the major features, physical and functional specifications, mounting and power requirements, the interface, and typical timing characteristics of the TM65 series of drives.

#### 1.2 PURPOSE OF THE DRIVE

These drives are rotating disk memories designed for random access data entry, storage, and retrieval applications. Typical applications include intelligent terminal controllers, microcomputers, word processing systems, data communication systems, error logging, microprogram loading, and point-of-sale terminals.

#### INTERNAL TRIM ERASE

The drive provides the control signals necessary for proper trim erasure of data.

#### INDUSTRY STANDARD INTERFACE COMPATIBILITY

The drive is compatible with controllers that use an industry standard interface.

#### ACTIVITY INDICATOR

An activity indicator, located on the front panel, is automatically illuminated when the drive is selected.

#### COMPACT SIZE

The reduced height of the drive enables it to occupy only one-half the mounting space required for a conventional drive.

### 1.3 MAJOR FEATURES

#### MICROPROCESSOR CONTROL

The TM65-4 drive features an onboard microprocessor, providing four major features:

1. Momentary motor start for improved media centering.
2. Improved head positioning accuracy with reduced hysteresis.
3. Write current switching for optimal recording quality.
4. Programmable Ready signal.

#### NOTE

Through the use of LSI circuitry, the microprocessor has been eliminated on the TM65-1L and TM65-2L.

#### WRITE PROTECT

When a write protected diskette is inserted in the drive, the write electronics are disabled.

#### DAISY CHAIN CAPABILITY

The drive provides the address selection and gating functions necessary to daisy chain a maximum of four units at the user's option. The last drive on the daisy chain terminates the interface. The terminations are accomplished by a resistor array plugged into a DIP socket.

### 1.4 FUNCTIONAL DESCRIPTION

The drives are fully self-contained, and require no operator intervention during normal operation. Each drive consists of a direct drive spindle motor, a head positioning system, and a read/write system.

When the front latch is opened, access is provided for insertion of a diskette. The diskette is held in place by aluminum guide rails. Its location is ensured when the diskette is inserted until a back stop is encountered and the ejection mechanism latches.

Closing the front latch on the TM65-4 activates the motor start circuit momentarily, resulting in accurate centering and clamping of the diskette. The drive hub on all versions is held at a constant speed of 300 RPM by a servo-controlled, direct drive, brushless D. C. motor. The heads remain in contact with the recording media until the front latch is opened. If media is not present and the front latch is closed, the heads will remain separated from each other on double-sided drives.

The heads are positioned over the desired track by means of a four-phase stepper/band assembly and its associated electronics. This positioner uses a one-step rotation for 96 TPI to cause a one track linear movement, and a two-step rotation for 48 TPI to cause a one track linear movement.

Data recovery electronics includes an integrated read amplifier, differentiator, zero crossover detector, and digitizing circuit. No data decoding capabilities are provided.

The drive has the following sensors:

1. An optical index sensor generates a digital signal when the index hole on the diskette is detected.
2. An optical write protect sensor disables the write electronics when a write protect tab is applied to the diskette.
3. A motor start switch provides momentary motor spin-up to help center the diskette when the front latch is closed (TM65-4 only).
4. An optical Track 0 sensor detects when the head/carriage assembly is positioned at Track 0.

## 1.5 PHYSICAL DESCRIPTION

A representative drive is shown in Figure 1-1. The drive can be mounted in a vertical or horizontal plane. However, the logic circuit board must be on the uppermost side when the drive is mounted horizontally.

The read/write head assembly is positioned by a split band positioner mounted to a stepper motor. The read/write heads are glass-bonded, ferrite/ceramic structures with a life expectancy of 20,000 operating hours.

Operator access for diskette loading is provided via a horizontal slot located at the front of the drive.

The electronic components of the drive are mounted on two printed circuit boards. The logic circuit board is mounted above the chassis. The motor control circuit board is mounted directly to the spindle motor. Power and interface signals are routed through connectors plugging directly into the logic circuit board.

The spindle is driven by a direct drive, brushless D.C. spindle motor with integral tachometer and speed control circuit. All of the electronics associated with the spindle motor are mounted on the motor itself. A 50 and 60 Hertz strobe pattern is printed directly on the motor, allowing visual verification of the motor's speed.

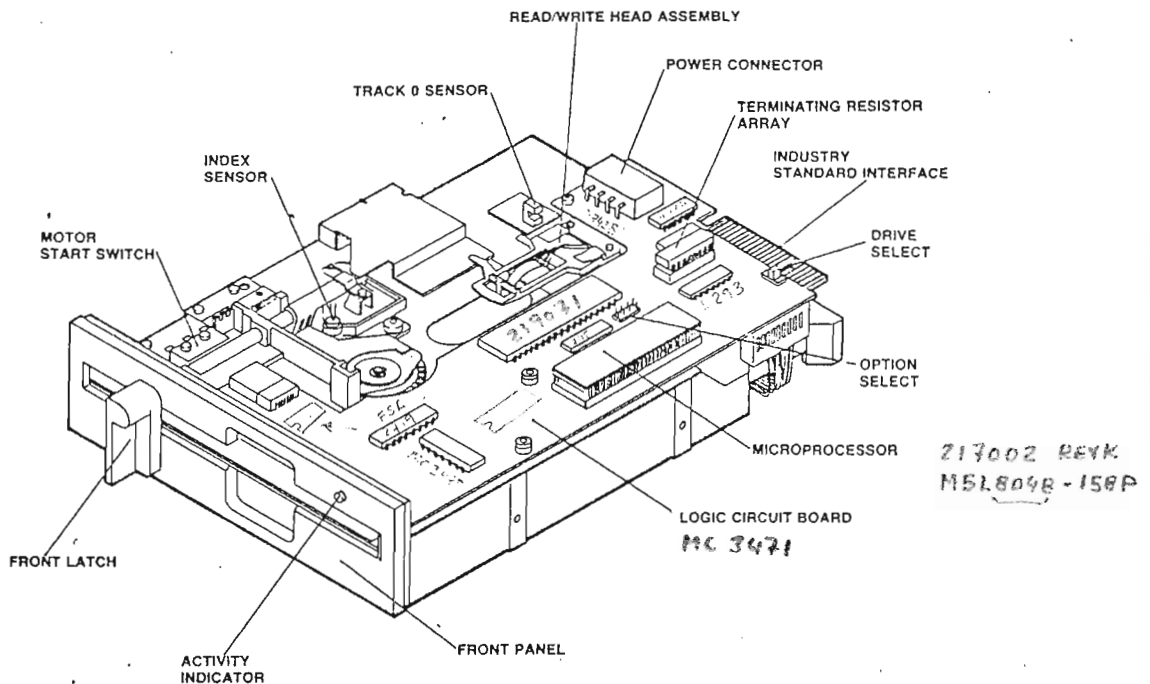


FIGURE 1-1  
TM 65-4 DISK DRIVE WITH HEAD SHIELD REMOVED

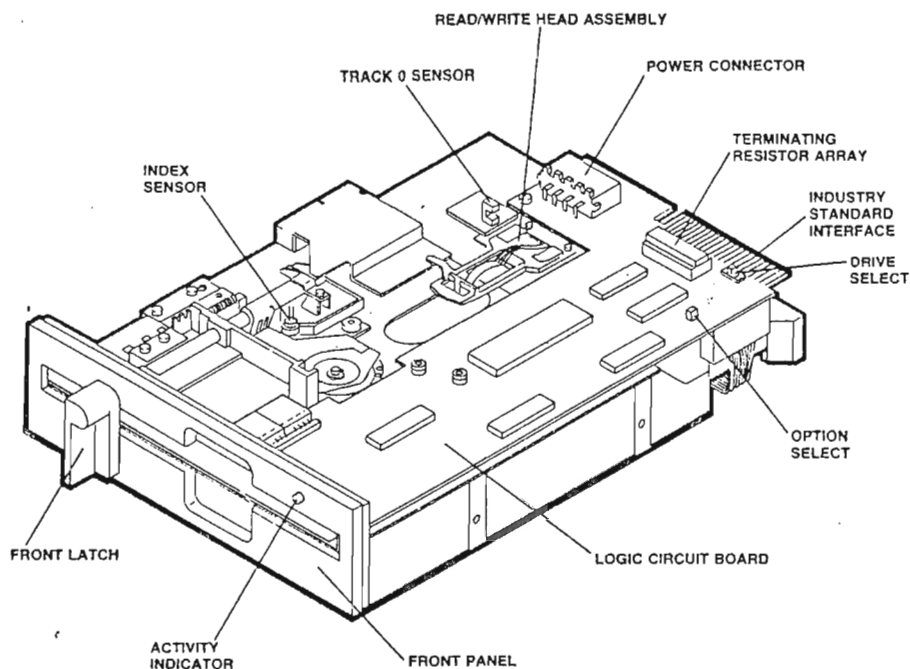


FIGURE 1-2

TM 65-2L DISK DRIVE WITH HEAD SHIELD REMOVED

## SECTION 2

# PRODUCT SPECIFICATIONS

### INTRODUCTION

This section contains the mechanical, electrical and operational, reliability, and environmental specifications for the TM65 series of disk drives.

#### 2.1 MECHANICAL SPECIFICATIONS

The physical dimensions of the drive are located in Figure 2-1.

#### 2.2 ELECTRICAL AND OPERATIONAL SPECIFICATIONS

The electrical and operational specifications are located in Table 2-1


#### 2.3 RELIABILITY SPECIFICATIONS

The reliability specifications are located in Table 2-2.

#### 2.4 ENVIRONMENTAL SPECIFICATIONS

The environmental specifications are located in Table 2-3.

This product is recognized under U.L. EMRT2, Component-Data Processing Equipment, Electronic.

 Certified



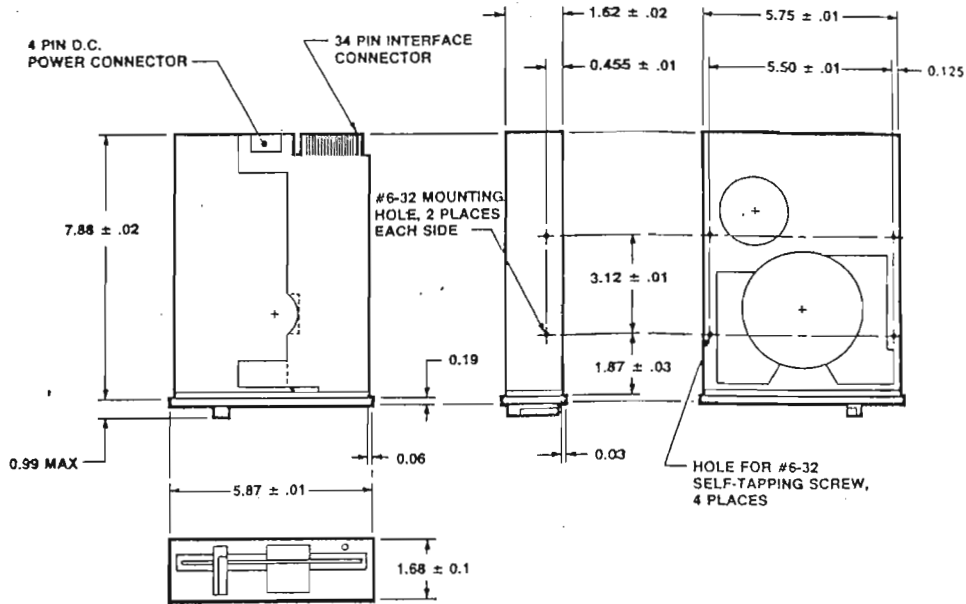


FIGURE 2-1  
DISK DRIVE OUTLINE DRAWING

NOTES: ALL DIMENSIONS ARE IN INCHES  
WEIGHT IS 2.62 POUNDS, 1.18 KILOGRAMS  
DOTTED LINE INDICATES LSI  
CIRCUIT BOARD OUTLINE

TABLE 2-1  
ELECTRICAL AND OPERATIONAL SPECIFICATIONS

Media	ANSI-compatible, 5-1/4-inch diskette
Media Life (For Reference Only)	4 x 10 <sup>6</sup> passes per track
Tracks Per Inch	
TM65-1L	48 TPI
TM65-2L	48 TPI
TM65-4	96 TPI
Tracks Per Drive	
TM65-1L	40 tracks
TM65-2L	80 tracks
TM65-4	160 tracks
Track Spacing	
TM65-1L	0.529 millimeters, 20.8 milinches
TM65-2L	0.529 millimeters, 20.8 milinches
TM65-4	0.265 millimeters, 10.4 milinches
Head Life	20,000 media contact hours
Disk Rotational Speed	300 RPM ± 1.5 percent
Average Rotational Latency	100 milliseconds
Instantaneous Speed Variation (ISV)	± 2 percent
Motor Start Time	250 milliseconds, maximum
Seek Time, track to track	
TM65-1L	6 milliseconds minimum
TM65-2L	6 milliseconds minimum
TM65-4	3 milliseconds minimum

TABLE 2-1 (CONTINUED)  
ELECTRICAL AND OPERATIONAL SPECIFICATIONS

Data Transfer Rate	250,000 bits per second, double density
Flux Reversals Per Inch (FRPI), inside track	
All Models, Side 0	5,535 FRPI
TM65-2L and TM65-4, Side 1	5,877 FRPI
Unformatted Recording Capacity, double density	
TM65-1L	250 kilobytes per disk
TM65-2L	500 kilobytes per disk
→ TM65-4	1 megabyte per disk
Shipment	When prepared for shipment by Tandon, the drive meets the requirements of NSTA pre-shipment test procedure Project 1A.
Head Settling Time	15 milliseconds
Average Track Access Time, including head settling time	90 milliseconds
Typical Recording Modes	FM, MFM, MMFM
D. C. Voltage and Current Requirements	
TM65-1L, TM65-2L	↓ TM65-4
+12 volts ± 0.6 volt at 500 milliamperes average, 1.0 amperes maximum, with less than 100 millivolts peak-to-peak ripple.	+12 volts ± 0.6 volt at 900 milliamperes average, with less than 100 millivolts peak-to-peak ripple.
	850 milliamperes maximum surge current if seek is not performed. If a seek is performed during the motor start interval, surge current is 1.15 amperes maximum for 150 milliseconds.
+5 volts ± 0.25 volt at 300 milliamperes average, 400 milliamperes maximum, with less than 50 millivolts peak-to-peak ripple.	+5 volts ± 0.25 volt at 450 milliamperes average with less than 50 millivolts peak-to-peak ripple.

TABLE 2-2  
RELIABILITY SPECIFICATIONS

Error Rates, maximum, exclusive of external sources, e.g.: electronics, defective, and contaminated diskettes	
Soft Errors (Recoverable)	One in 10 <sup>9</sup> bits
Hard Errors (Nonrecoverable)	One in 10 <sup>12</sup> bits
Seek Errors	One in 10 <sup>6</sup> seeks
Mean Time Between Failures	11,000 hours, 100 percent duty cycle
Mean Time To Repair	30 minutes

TABLE 2-3  
ENVIRONMENTAL SPECIFICATIONS

Temperature	
Operating, Media Dependent	10°C to 46°C, 50°F to 115°F
Nonoperating	-40°C to 71°C, -40°F to 160°F
Relative Humidity	
Operating, noncondensing, Media Dependent	20-to-80 percent
Nonoperating, noncondensing	5-to-95 percent
Altitude	
Operating or Nonoperating	152.4 meters, 500 feet, below sea level, to 15,240 meters, 50,000 feet, above sea level

## SECTION 3

# OPERATION

### INTRODUCTION

This section contains information on how to unpack, check out, install, and operate the TM65 series of drives.

#### 3.1 UNPACKING THE DRIVE

The drives are shipped in protective containers to minimize the possibility of damage during shipment. The following list is the recommended procedure for unpacking the drive.

1. Place the container on a flat work surface, top side up.
2. Cut the tape that holds the tab in the slot on the front side of the container.

#### CAUTION

*Container may spring open when the tape is cut.*

3. Remove drive from plastic bag.
4. Inspect the drive for possible damage.
5. Notify the carrier immediately if any damage is found.
6. Save the shipping container for future use.

#### 3.2 PREINSTALLATION CHECKOUT

Before applying power to the drive, the following inspection should be conducted:

1. Remove the cardboard shipping insert, and retain for future shipment.

#### CAUTION

*Turning the front latch to the open position will cause the shipping insert to eject. Remove the insert slowly to prevent damage to the upper slider.*

2. Check to ensure that the front latch rotates easily. It should remain in the open position when rotated fully counterclockwise (horizontal to front panel).
3. When the latch is moved to an open position, the head arm raises.
4. Ensure the front panel is secure.
5. Manually rotate the drive hub. It should rotate freely.
6. Ensure both circuit boards are secure.
7. Ensure the connectors are firmly seated.

#### 3.3 MOUNTING THE DRIVE

The drive has been designed to be mounted horizontally or vertically. When mounted horizontally, the logic circuit board side of the drive must be the top side.

Two 6-32 tapped mounting holes are provided on each side and four holes for self tapping screws are provided on the bottom of the drive for attachment to user-supplied mounting brackets. When installed in either plane, horizontal or vertical, only two mounting screws are required to securely hold the drive in place. Under no circumstances should four or more mounting screws be used.

Two drives may be mounted in a single, full-size drive enclosure, 3.25-inches high. A two-hole mounting scheme per drive is recommended for mounting in a two drive configuration.

Any mounting scheme in which the drive is part of the structural integrity of the enclosure is not permitted. Mounting schemes should allow for adjustable brackets or incorporate resilient members to accommodate tolerances. In addition, it is recommended that mounting schemes include no more than two mounting surfaces.

The drive is manufactured and tested with some critical internal alignments that must be maintained. Hence, it is important that the mounting hardware not introduce significant stress on the chassis.

#### DUST COVER

The design of an enclosure should incorporate a means to prevent contamination from loose items, e.g., dust, lint, and paper chad since the drive does not have a dust cover.

#### COOLING

Heat dissipation from a single drive is normally 9 watts, 31 BTU per hour for the LSI version and 13 watts, 44 BTU per hour for the microprocessor version under high load conditions. When the drive is mounted so the components have access to a free flow of air, normal convection cooling allows operation within the specified temperature range.

When forced air is used, air flow must be directed outward from the drive. Do not intake air through the drive or heads and diskettes.

The use of forced air flow is recommended when two drives are mounted within a single enclosure.

### 3.4 INTERFACE CONNECTIONS

Interface connections for the TM65 series drives are made via a user-supplied, thirty four-pin, flat ribbon connector, 3M Part Number 3463-0001 or AMP Part Number 583717-5, using contact Part Number 1-583616-1 for twisted pair or its equivalent. This connector mates directly with the circuit board connector at the rear of the drive.

The D. C. power connector is a four-pin connector located at the rear of the drive. The interface description of the connectors, and the location of each one, is contained in this section. Interface lines are located in Table 3-1. D. C. power connector pin assignments are located in Table 3-2, Page 3-7.

The signal wire harness should be of the flat ribbon or twisted pair type, 26-to-28 gauge conductor, compatible with the connector to be used. The recommended cable length is ten feet maximum.

TABLE 3-1 DRIVE INTERFACE LINES AND PIN ASSIGNMENTS		
Input Control Lines: Controller-To-Disk Drive		
Ground	Pin	Signal
1	2	Spare
3	4	Spare
5	6	Drive Select 3
9	10	Drive Select 0
11	12	Drive Select 1
13	14	Drive Select 2
15	16	Motor On
17	18	Direction Select
19	20	Step
21	22	Composite Write Data
23	24	Write Enable
31	32	Side Select
Output Control Lines: Disk Drive-To-Controller		
Ground	Pin	Signal
7	8	Index/Sector
25	26	Track 0
27	28	Write Protect
29	30	Composite Read Data
33	34	Ready*

\*TM65-4 Standard, see Table 3-3. TM65-2L Optional. Contact your Tandon representative.

#### INPUT CONTROL LINES

#### DRIVE SELECT LINES

The Drive Select lines provide a means of selecting and deselecting a drive. These four lines select one of the four drives attached to the controller.

When the signal logic level is true (low), the drive electronics are activated, then the drive is conditioned to respond to Step or Read/Write commands. A Drive Select line must remain stable in the true (low) state until a Step or Read/Write command is completed. When the signal line logic level is false (high), the input control lines and output status lines are disabled.

The drive address is determined by a jumper select on the logic circuit board. Drive select lines 0 through 3 provide a means of daisy chaining a maximum of four drives to a controller. Only one can be true (low) at a time. An undefined operation results if two or more drives are assigned the same address or if two or more Drive Select lines are in the true (low) state simultaneously.

#### MOTOR ON

When this signal is true (low), the drive motor accelerates to its nominal speed of 300 RPM, and stabilizes at this speed in less than 250 milliseconds. When the signal line logic level goes false (high), the drive decelerates to a stop. This signal may be gated with Drive Select as an option.

On the TM65-4, the motor activates momentarily when the front latch is closed. This motor start function remains active for approximately three seconds, unless Motor On is in the true (low) condition.

#### DIRECTION SELECT AND STEP LINES (TWO LINES)

When the drive is selected, a true (low) pulse on the Step line, with a time duration greater than 200 nanoseconds, initiates the access motion. The direction of motion is determined by the logic state of the Direction Select line when a step pulse is issued. The motion is toward the center of the disk if the Direction Select line is in the true (low) state. The direction of motion is away from the center of the disk if the Direction Select line is in the false (high) state.

To ensure proper positioning, the Direction Select line should be stable at least 100 nanoseconds prior to issuing a corresponding step pulse, and remain true (low) 100 nanoseconds after it.

The access motion is initiated on the trailing edge of the step pulse. The time period between consecutive trailing edges of step pulses should be three milliseconds for the TM65-4 and six milliseconds for the TM65-1L and TM65-2L.

The drive must be stepped at either three or six milliseconds, depending upon the jumper options. If selection of other step rates is desired, consult your local Tandon representative.

The drive electronics ignore step pulses when one of the following conditions exists:

1. The write enable is true (low).
2. The direction select is false (high), and the head is positioned at Track 0.
3. The drive is not selected.
4. When trying to seek beyond Track 79 on the TM65-4.
5. When the door latch is opened on the TM 65-4.

## COMPOSITE WRITE DATA

When the drive is selected, this interface line provides the bit serial composite write data pulses that control the switching of the write current in the selected head. The write electronics must be conditioned for writing by the Write Enable line.

For each high-to-low transition on the Composite Write Data line, a flux change is produced at the write head gap. This causes a flux change to be recorded on the media.

The microprocessor on the TM65-4 automatically decreases write current by 25 percent, when writing on the inner tracks, for optimal recording quality. Write current is switched at Track 40.

When a single-density (FM) type encoding technique is used in which data and clock form the combined Write Data signal, it is recommended that the repetition of the high-to-low transitions, while writing all zeros, be equal to one-half the maximum data rate, 125 kilohertz  $\pm 0.1$  percent, and the repetition of the high-to-low transitions, when writing all ones, be equal to the maximum data rate, 250 kilohertz  $\pm 0.1$  percent.

Host controllers may implement write precompensation circuits that recognize worst case patterns and adjust the write data waveform. Although a value cannot be specified for write precompensation, Tandon suggests a value of 250 nanoseconds for systems using MFM double density recording format.

### WRITE ENABLE

When this signal is true (low), the write electronics are prepared for writing data and the read electronics are disabled. This signal turns on write current in the selected read/write head. Data is written under the control of the Composite Write Data and Side Select input lines. When the Write Enable line is false (high), all write electronics are disabled.

When a write protected diskette is installed in a drive, the write electronics are disabled, irrespective of the state of the Write Enable or Side Select lines.

### SIDE SELECT, TM65-2L AND TM65-4

The Side Select interface line defines which side of a two-sided diskette is used for information transfer.

A false (high) level on this line selects the read/write head on side zero, the lower head, of the drive. A true (low) level on this line selects the read/write head on side one, the upper head, of the drive. Side Select is ignored by the TM65-1L.

## OUTPUT CONTROL LINES

### INDEX/SECTOR

The index/sector signal is a composite of the index pulse and sector signals.

An index pulse is provided once every revolution, 200 milliseconds nominal, to indicate the beginning of a track to the controller. The leading edge of this signal must always be used to ensure timing accuracy. The index/sector line remains in the true (low) state for the duration of the index pulse, which is nominally four milliseconds.

The sector signal portion appears only when using hard sectored diskettes.

### TRACK 0

When the drive is selected, the Track 0 interface signal, when true (low), indicates to the controller that the read/write heads are positioned on Track 0. This signal remains true (low) until the heads are moved from Track 0.

### WRITE PROTECT

When the Write Protect line goes true (low), the diskette is write protected and the write electronics are disabled. It is recommended the controller not issue a Write command when the Write Protect signal is true (low).

When the Write Protect line is false (high), the write electronics are enabled.

### COMPOSITE READ DATA

This interface line transmits the readback data to the controller when the drive is selected. It provides a pulse for each flux transition detected from the diskette. The Composite Read Data output line goes true (low) for a duration of  $1 \pm 0.25$  microsecond for each flux change detected from the diskette.

The leading edge of the Composite Read Data output pulse represents the true position of the flux transitions on the diskette's surface.

**READY, TM65-4 ONLY**

The Ready signal indicates the operational status of the drive. There are two ready signal conditions selectable by use of programming jumper connectors (see Section 3.6).

Ready is defined as drive selected and door closed only, or drive selected, door closed, diskette inserted and up to speed. Diskette inserted means that at least one index pulse has been detected. Up to speed means that 250 milliseconds have elapsed since the motor has been turned on. Ready goes false when the motor is turned off or the door is opened.

**TYPICAL INTERFACE CHARACTERISTICS**

Lines between the controller and the drive have the following characteristics:

$$V_{out} \text{ True} = +0.4 \text{ volt maximum at } I_{out} = 48 \text{ milliamperes, maximum}$$

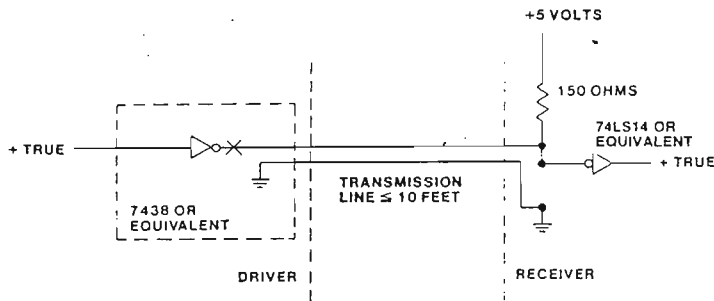
$$V_{out} \text{ False} = +2.4 \text{ volts minimum open collector at } I_{out} = 250 \text{ microamperes, maximum}$$

Figure 3-1 contains the characteristics of the electrical interface. Figure 3-2 contains the control and data timing requirements.

**3.5 D. C. POWER**

D. C. power is supplied to this drive via a four-pin AMP connector, J2, mounted on the logic circuit board. The mating connector, not supplied, is AMP Part Number 1-480424-0, using AMP contact Part Number 60619-1. Pin assignments are found in Table 3-2.

The chassis should be connected to earth ground to ensure proper operation. The conductor should be 16-to-18 AWG, minimum.



**FIGURE 3-1  
ELECTRICAL INTERFACE CHARACTERISTICS**

TABLE 3-2 D. C. POWER CONNECTOR PIN ASSIGNMENTS	
Pin	Supply Voltage
1	+ 12 volts D. C.
2	Common D. C. return
3	
4	
Pin	Signal
Ground lug 3/16-inch quick disconnect	Chassis ground from controller

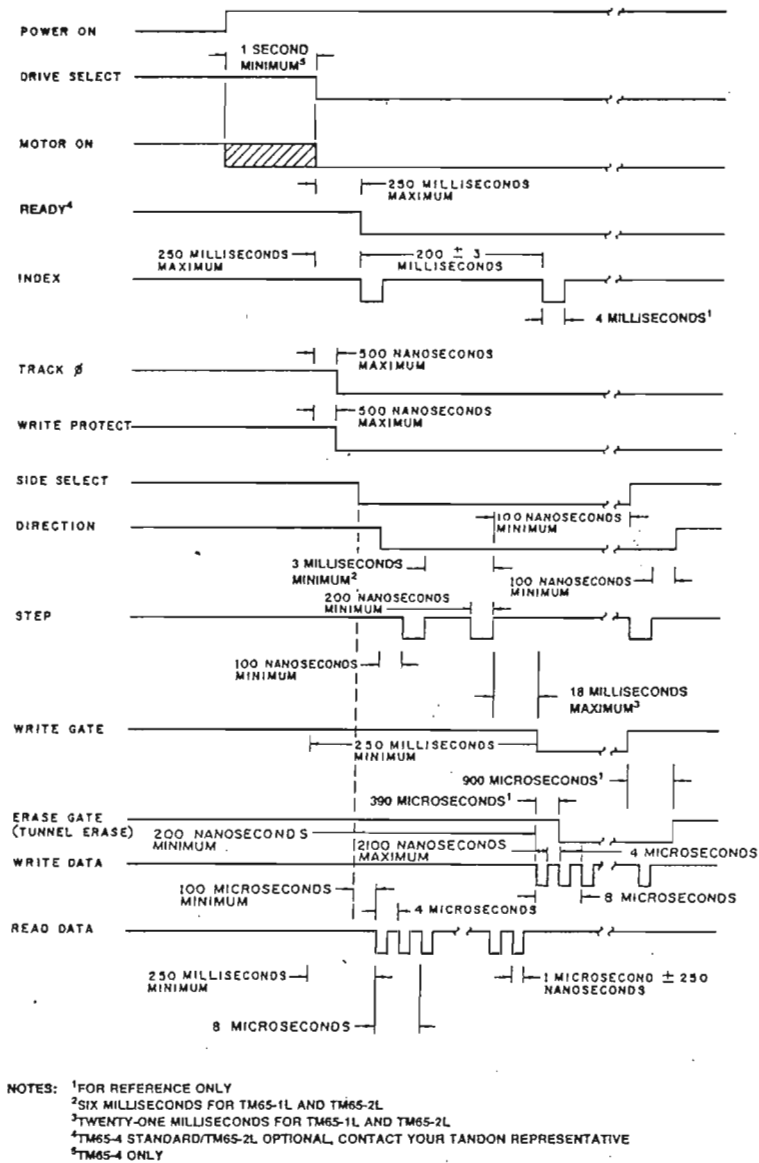


FIGURE 3-2  
CONTROL AND DATA TIMING REQUIREMENTS

### STEPPER MOTOR POWER SAVE (TM65-4)

The +12 volts is applied to the stepper motor only while stepping. This voltage is reduced to +5 volts, 50 milliseconds after the last step has been completed.

In order to conserve peak power in the system, the stepper motor power is delayed when the spindle motor is first turned on unless a seek operation is requested at this time.

### RESTORE

The Restore operation on the TM65-4 returns the heads to Track 0 during the power up sequence. Restore operation on the TM65-1L and TM65-2L is accomplished by the host controller.

### 3.6 DRIVE ADDRESS AND OPTION PATCHING

The drive address and option patching is determined by the different jumper configurations required for specific system applications. If jumper configurations are changed on the TM65-4, power should be cycled off and on so the microprocessor can recognize the new configuration.

### DS0 THROUGH DS3 JUMPERS (ALL DRIVES)

This option allows the user to daisy chain up to four drives, and to enable one drive at a time. Drive Select is implemented by shorting one of the four connections, using a shorting plug.

The terminator resistor pack, RPI, located on the logic circuit board should be installed in the last drive of the daisy chain (Figure 3-3, 3-4). All other devices on the interface must have the resistor pack removed.



**S1 THROUGH S4 OPTION JUMPERS (TM65-4)**

Disk drive configurations are available via jumper options S1, S2, S3, and S4. A specific combination of 16 bits define a configuration. If an unused configuration is jumpered, the Front Panel L.E.D. blinks until the power is turned off and a defined configuration is jumpered (Figure 3-3).

All options do automatic centering while the latch is being closed.

Table 3-3 shows the options available. An X denotes jumper installation, and a dash (-) denotes jumper removed.

**NOTE**

The ready signal, with the door closed and one index pulse detected, is delayed 250 milliseconds after power on (after 1 second delay).

If jumper configurations are changed, power should be cycled off and on so the microprocessor can recognize the next configuration.

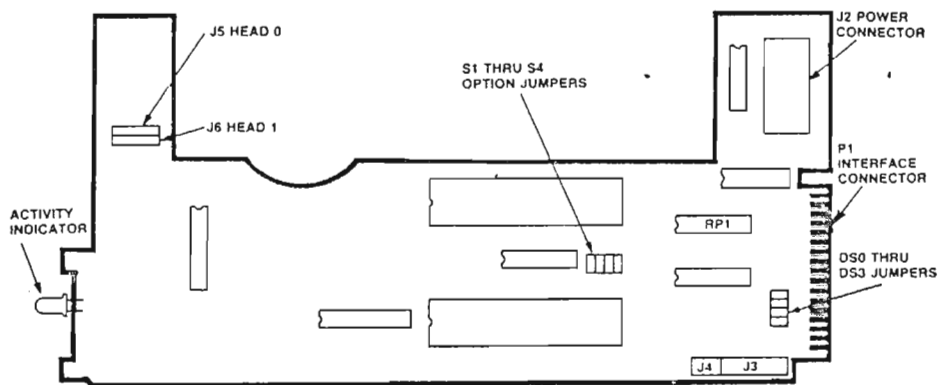
**TABLE 3-3  
TM65-4 OPTIONS**

S1	S2	S3	S4	Ready Is A Function Of:	Drive Motor On Is A Function Of:	Motor Off Delay
-	-	-	X	Door Closed, up to speed and drive selected	Drive Select or Motor On	None
-	-	X	-	Door Closed, up to speed and drive selected	Drive Select and Motor On	None
-	X	-	-	Door Closed, up to speed and drive selected	Motor On	3 seconds
-	X	X	-	Door Closed, up to speed and drive selected	Motor On	None
X	-	-	-	Door Closed and drive selected	Drive Select and Motor On	None
X	-	-	X	Door Closed up to speed and drive selected	Drive Select or Motor On	3 seconds
X	-	X	X	Door Closed and drive selected	Motor On	3 seconds
X	-	X	-	SELF SEEK CYCLE, 3 Millisecond Step Rate		

CONEXION

NOTE: Motor stops when door is opened:

40 PISMS



**FIGURE 3-3  
LOGIC CIRCUIT BOARD OPTION LOCATIONS, TM65-4**

**JP2 AND JP7 OPTION JUMPERS  
(TM65-1L, TM65-2L)**

Disk drive configuration options are provided by JP2 and JP7 (Figure 3-4).

**DRIVE SELECT CONTROL (JP2)**

The JP2 jumper is used only in single drive systems when the user requires the drive logic to be enabled at all times. The DS0 through DS3 Drive Select lines are disabled with JP2 installed, eliminating need for the host controller to issue a Drive Select signal.

**JP2 DRIVE SELECT CONTROL**

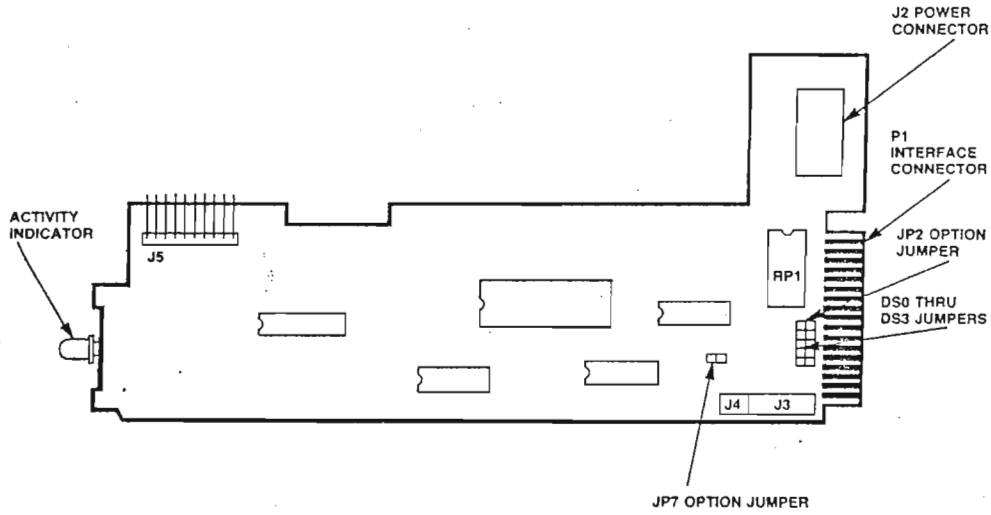
- X Drive Selected at all times.
- Drive Select controlled by DS0 through DS3.

**MOTOR ON CONTROL (JP7)**

Connecting JP7, A to C, allows spindle motor control via J1, pin 16. If the B to C jumper is installed, the spindle motor is controlled by Drive Select.

**C-A C-B MOTOR CONTROL**

- X — Spindle motor controlled by Motor On signal
- X Spindle motor controlled by Drive Select.



**FIGURE 3-4  
LOGIC CIRCUIT BOARD OPTION LOCATIONS  
TM65-1L, TM65-2L**

### 3.7 DISKETTES

The TM65 series of drives use an ANSI-compatible 5-1/4-inch diskette. Diskettes are available with a single index hole or with multiple (index and sector) holes. The TM65-4 drive requires the use of 96 TPI certified media. Use of other media results in poor data reliability.

Diskettes with a single hole are used when soft sector format is required. Multiple hole diskettes provide sector information through the use of an index sensor and electronics.

Figure 3-5 illustrates the diskette used with the drive. This recording media is a flexible diskette enclosed in a protective jacket. The protected diskette, free to rotate within the jacket, is continuously cleaned by its soft fabric lining during normal operation.

#### LOADING THE DISKETTE

The drive is loaded by inserting the diskette, head aperture forward, into the front slot of the

drive. Access to the diskette loading slot is obtained by opening the front latch.

The diskette should be carefully inserted until it is solidly against the back stop.

#### CAUTION

*Damage to the center of the diskette may result if the door is closed when the diskette is not properly inserted. This prevents reliable recovery of the recorded data.*

#### WRITE PROTECT TAB

The drive is equipped with a Write Protect Sensor Assembly. This sensor operates in conjunction with a diskette that has a slot cut in the protective jacket. Figure 3-5 contains the location of the slot.

When the slot is covered with an optically opaque self-adhesive tab, the diskette is write protected. The tab must be removed to write on the diskette. Figure 3-6 contains information on how to install a tab to cover the slot.

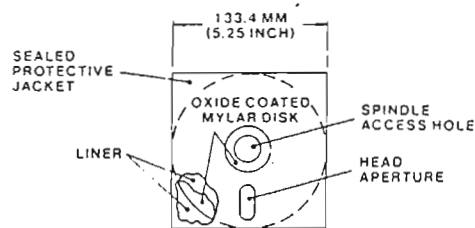
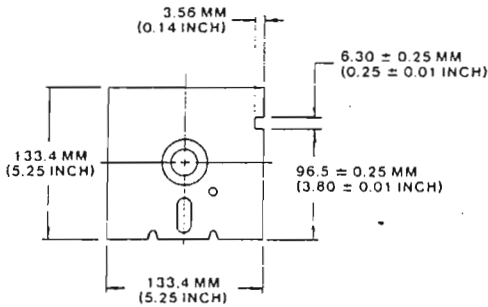


FIGURE 3-5  
RECORDING MEDIA

#### DISKETTE HANDLING AND STORAGE

It is important the diskette be handled and stored correctly so the integrity of the recorded data is maintained. A damaged or contaminated diskette can impair or prevent recovery of data, and can result in damage to the read/write heads.

Figure 3-6 contains an illustration of the physical configuration of the diskette. The 5-1/4-inch diskette is oxide-coated, flexible mylar. It is enclosed in a 5-1/4-inch square protective jacket. Read/write head access is made through an aperture in the jacket. In addition, openings for the drive hub and diskette index hole are provided.

Figure 3-7 provides some helpful hints on the care and handling of the drive and diskettes. In addition, to ensure trouble-free operation and to enhance the service life of the diskette, the

following handling procedure should be observed.

1. Return the diskette to the protective jacket when not in use.
2. Avoid exposing the diskette to any magnetizing force in excess of 50 oersted.

#### NOTE

The 50-oersted level magnetizing force is reached at a distance of approximately three inches from a typical source, e.g., motors, generators, or transformers.

3. To avoid warping, do not store the diskette in direct sunlight.
4. Do not use a lead pencil or a ballpoint pen to write on the label. Use a felt tipped pen, and mark lightly on the label.

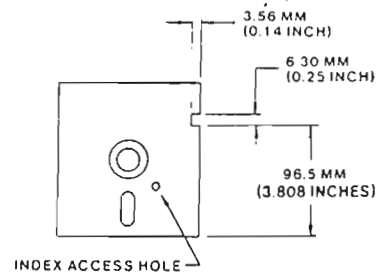
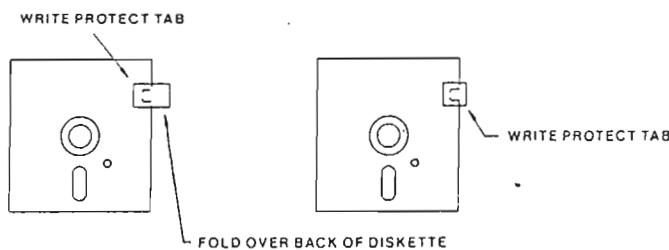
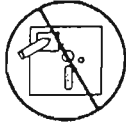
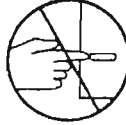


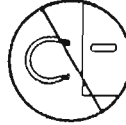
FIGURE 3-6  
WRITE PROTECT TAB



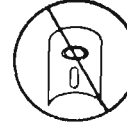
DO NOT WRITE ON THE JACKET WITH PEN OR PENCIL. USE A FELT TIPPED PEN.



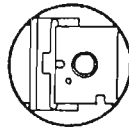
DO NOT TOUCH PRECISION SURFACE WITH YOUR FINGERS.



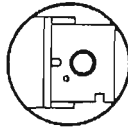
KEEP THE DISKETTE AWAY FROM MAGNETIC FIELDS.



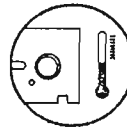
HANDLE WITH CARE: BENDING AND FOLDING MAY DAMAGE DISKETTE.



TO AVOID DAMAGE TO THE DISKETTE AND TO YOUR DRIVE, INSERT DISKETTE CAREFULLY UNTIL THE BACKSTOP IS ENCOUNTERED.



RETURN THE DISKETTE TO ITS JACKET WHEN NOT IN USE.



DISKETTES SHOULD BE STORED AT 10°C TO 52°C 50°F TO 125°F

FIGURE 3-7  
DISKETTE CARE AND HANDLING